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APRIL 2005 • Volume 9 Number 3

Sizing up 3U for JTRS Cluster 4

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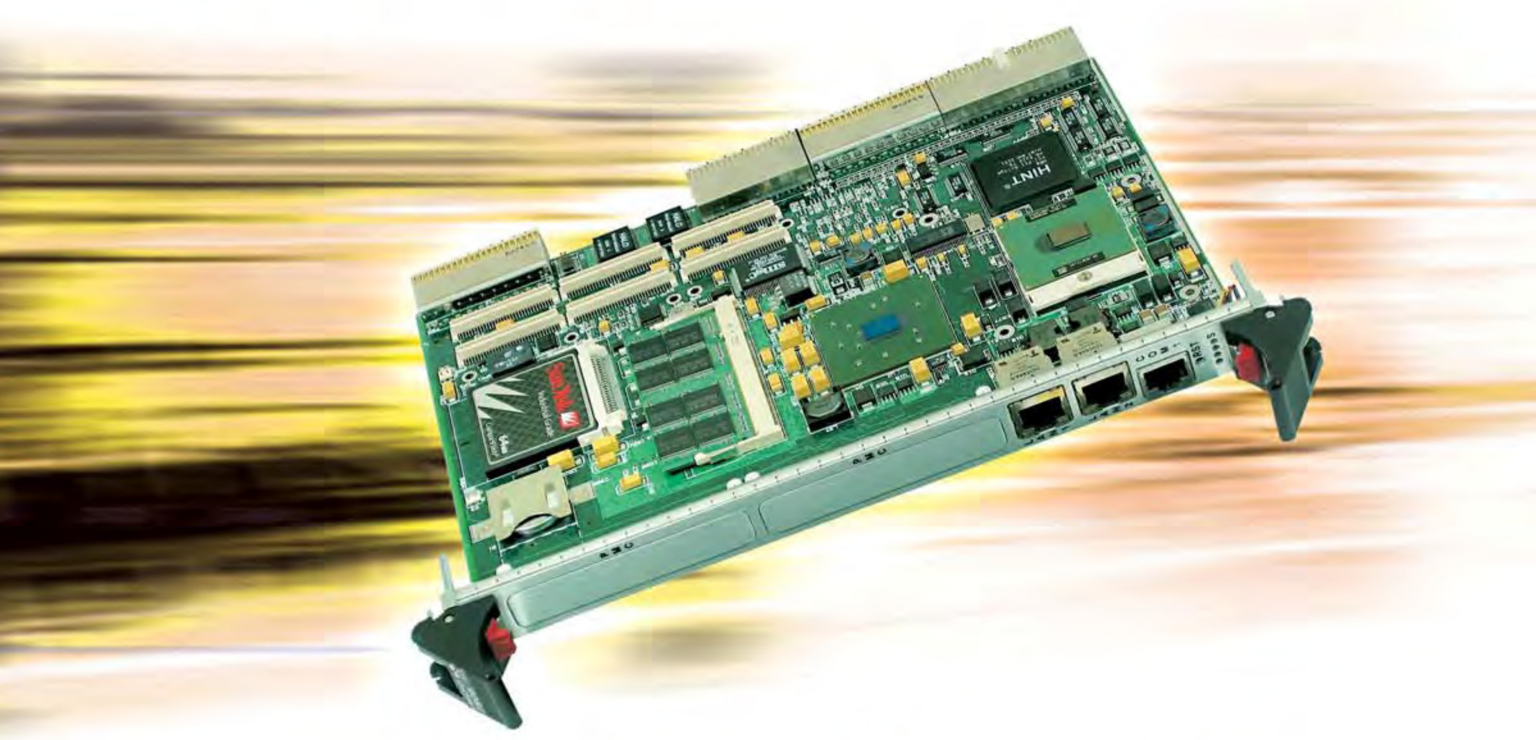

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EDITOR'S FOREWORD

Staying cool

By Joe Pavlat
Editorial Director

CompactPCI & AdvancedTCA

The bounty of Moore's Law is something hardware engineers, software developers, and consumers tend to take for granted. Every year or so we're handed faster processors, more powerful peripherals, and bigger and faster memory. Hardware components just get quicker and cheaper. Software development also benefits hugely from Moore's Law. As someone once said, "what the hardware guys giveth the software guys taketh away" has led to ever more powerful software that can be written somewhat inefficiently and still perform well. Life is good. I often wish the growth of my investments year to year would follow Moore's Law. Fat chance.

There is an emerging problem, however, that may practically slow future improvements, and it is fundamental. Keeping gigahertz processors and gigabytes of memory cool enough to perform reliably is becoming more and more difficult. Electronic systems transfer heat three ways: convection, conduction, and radiation.

Convective air cooling has always been the backbone of commercial, industrial, medical, and telecom equipment. While conduction cooling and other exotic and expensive cooling technologies are used in niche applications, notably military and avionics equipment, air cooling is the primary method for cooling any piece of equipment dissipating more than a few dozen watts. Electromechanical fans and blowers have been used for 50 years to do this, and they continue to be the basic technology of choice. Although fan performance continues to improve, industry studies show it improving at a maximum of 5-10 percent per year. That improvement rate just can't keep up with semiconductors' 50+ percent annual growth in speed and transistor count that continues to demonstrate Moore's Law. It is true that semiconductors become somewhat more thermally efficient as feature size and operating voltage decrease. However, those improvements are relatively small and are becoming less so every year. When all is said and done, semiconductor die must be maintained at a temperature below the junction temperature of silicon or failure will occur. As operating temperature rises, reliability decreases not just for silicon, but also for a wide range of electronic components.

Looking at some popular and emerging technologies helps illustrate the issue. Chassis for popular 6U 0.8-inch pitch technologies like CompactPCI and VME can dissipate a maximum of about 1 watt per cubic inch of board volume. This number does not include the additional volume required for ingress and egress air plenums, so the effective dissipation for the entire chassis is probably 20-30 percent less than that. After extensive thermal modeling using sophisticated computational fluid dynamics and thousands of hours of computer time, the specialists developing the thermal specifications for AdvancedTCA were able to improve the board volume dissipation to about 1.25 watts per cubic inch. And even that modest improvement requires very careful board and chassis design to ensure unimpeded and even airflow. Component placement and airflow impedance are important considerations for board design and layout. Simply installing bigger and bigger fans often does not improve the situation unless airflow can truly be increased over hot components. Even a lightly loaded chassis can cause boards to overheat if the majority of air ends up moving through empty slots. Also the acoustic noise produced by big fans and blowers can run afoul of NEBS and OSHA safety requirements.

This issue isn't going away. Our industry needs to proactively address this problem and create not just point solutions, but rather open industry standards that will drive a large number of vendors to provide standardized, inexpensive, and general solutions. Engineers and physicists must think outside the box and explore liquid cooling, spray cooling, and conduction cooling technologies. Working towards developing standardized solutions that can be purchased off-the-shelf and written into open standards is key.

"The limit to the future of electronics is not Moore's Law; it's cooling Moore's Law. There are new ideas and techniques emerging for cooling densely packed electronics at the chip, board, and chassis level. And, many applications from telecom to military are looking for cooling methods more efficient than the traditional conduction or convection cooling techniques used today," said Ray Alderman, Executive Director of the VME International Trade Association (VITA) recently.

VITA has begun exploring some next generation technologies and is sponsoring a new conference devoted to the subject on May 17, 2005 as part of the May 16-17, 2005 MEECC conference in Long Beach, CA. Information about the CoolCon Conference is available on the VITA website, www.vita.com. This is a good start. Over the next few years this issue will become more pressing, requiring the attention of the entire industry. It is a fascinating problem, and I hope to see innovative general solutions emerge in the coming years.

Joe Pavlat

Joe Pavlat
Editorial Director

Space savings spotlight rugged 3U CompactPCI

By Jacob Sealander

In this article Jacob discusses twin factors that are bringing 3U CompactPCI front and center for rugged systems, the drive to make ever more efficient use of real estate, and the need to shrink system weight.

While 6U cards remain the outstanding choice for most embedded defense and aerospace applications, in some very specific instances the 3U form factor clearly has a role to play. Two current trends, working in concert, are helping to create opportunities where rugged 3U CompactPCI systems can provide a viable alternative to the larger and more popular 6U systems. The first of these trends is the pressure to reduce space consumption. As vehicles such as helicopters, tanks, and Unmanned Aerial Vehicles (UAVs) carry an increasing array of electronics systems, the reduced space in these already space-limited environments drives further attempts to reduce the size of electronics systems. Meanwhile the expectations of increased performance and functionality demand that more compute power be delivered in the increasingly smaller enclosures. The second leading trend is the push to reduce system weight. This is especially true on space constrained tactical vehicles and is also becoming an issue for smaller UAVs, where the weight of the processing system has a direct impact on flight duration: the less weight, the longer fuel lasts and the longer reconnaissance missions stay aloft. Another program for which 3U CompactPCI is being considered is the next-generation Joint Tactical Radio System (JTRS). The airborne JTRS development subprogram, designated Cluster 4, is expected to be deployed on more than 65 different aircraft types, including rotary-wing and fixed-wing platforms such as the Marine Harrier (Figure 1).

Enter 3U

One reason that 6U cards, well established as the most popular board standard for embedded defense and aerospace applications, have proven so popular is that they provide sufficient board *real estate* to deploy large amounts of chip functionality. In addition, they support flexible system expansion via onboard PMC slots. In applications where space reduction is an issue, 3U cards, which measure 100mm x 160mm, less than half the width of 233mm x 160mm 6U cards, can provide an attractive alternative.

As space aboard aircraft and ground vehicles increasingly becomes a premium, the pressure to reduce overall system size increases. However addressing this issue has become easier as chip densities have increased and the use of large gate count FPGAs has continued to grow. It is now possible to deploy an increasing level of board functionality on smaller form factor cards, thus making up for some of the lost real estate. The system designer who prefers the smaller 3U form factor boards can gain an additional ruggedization benefit from 3U's significantly greater stiffness. This stiffness makes 3U boards potentially less susceptible to the destructive effects of shock and vibration. Vibration makes electronics components fail due to the flexing of the Printed Wiring Board (PWB). PWB flexes can strain the leads and solder joints of the electronic components. Over time, the board's solder joints and component leads can suffer fatigue fractures and ultimately cause board failure. Rugged boards are designed to minimize the flexing caused by vibration. The stiffer a board, the greater its ability to withstand shock and vibration. One indicator of a board's ability to survive significant vibration is the natural frequency of the card. A 3U card, being smaller, is naturally stiffer than a 6U card. All objects have a natural frequency and it is at that natural frequency that resonance and displacement are at their maximum. The higher the natural frequency, the greater the environmental vibration required to induce

Figure 1

destruction of the electronics. A well constructed, conduction-cooled 6U card has a natural frequency of 300-350 Hz, while 3U cards typically have a natural frequency ranging from 800-1000 Hz. Curtiss-Wright Controls Embedded Computing (CWCEC) has measured its 3U modules to have a natural frequency of more than 800 Hz, which translates into high reliability over the service life of the card. This allows systems to be mountable in especially hostile locations in vehicles, such as in close vicinity to guns and jet engines. For applications in which vibration will likely exceed 0.1 g2/Hz, the stiffer 3U boards are especially attractive.

When 6U boards prove too large for a given application, 3U CompactPCI cards can provide the ideal alternative. They combine several attractive features, including the space and ruggedization benefits discussed above, well suited for defense and aerospace applications. For one, 3U CompactPCI share the same plug-in module, passive backplane approach of 6U CompactPCI, with a blade and fork connector system that has proved itself reliable in high shock and vibration environments. Another advantage for MIL applications is the placement of all I/O signals at the backplane connector. Elimination of I/O on the front panel simplifies and speeds system maintenance. Repairs can be made more quickly since replacing a module doesn't involve the time-consuming removal and reinstallation of a cable harness.

Cooling simplified

Cooling can also be simpler with 3U cards. In a conduction-cooled card, the heat conduction from the electronic components is guided through the metal of the frame and the copper within the PWB to the side of the card where it then transfers into the chassis. Both 6U and 3U cards share the same 160 mm side dimension where this final transfer takes place. Since a 3U card will usually have fewer components onboard it will typically require less power than a 6U card. The 3U card has a further advantage in that the average distance from component to cooling edge is lower, thus incurring lower thermal resistance and, again, resulting in lower component temperatures.

A COTS tactical subsystem

To address increasing demands for high performance processing in applications with severe space constraints, CWCEC has developed a COTS based compact 3U CompactPCI off-the-shelf rugged computing system. Packaged in a battle ready rugged half-short five-slot Air Transport Rack (ATR) chassis, the 3U CompactPCI based Modular Tactical Computer (MTC) represents a significant step forward in the incorporation of mission-critical computing into military platforms. See Figure 2.

MTC offers defense and aerospace system integrators a complete COTS tactical subsystem that can be ordered off-the-shelf fully configured for immediate integration into a production application. Alternately, the MTC can be customized with a wide variety of functional modules to meet specific applications such as mission computing, control applications,

Figure 2

fire control systems, or network-centric computing. The MTC is factory configured with standard COTS boards and subassemblies based on open architecture technology.

At the core of MTC is CWCEC's DCP-122 3U CompactPCI single board computer, driven by an 800 MHz IBM 750FX processor. Processing performance for the MTC is rated at 1856 Dhrystone Millions of Instructions Per Second (DMIPS). MTC's standard configuration includes 256 MB of ECC DRAM, Ethernet, a tri-channel dual redundant 1553 bus, and nine serial channels (Sync/Async). The MTC can also be configured with either a Gigabit Ethernet switch or a 50 ms power holdup. Additional data communications functionality in the system includes 20 digital/analog input channels and converters. MTC is designed to PICMG 2.16 rev. 1.0 and supports packet-switching backplanes.

MTC is suitable for applications with severe space constraints. This new small, lightweight rugged computer system is designed to withstand the harsh environments of military missions. The MTC uses the same advanced cooling fin geometry found on 6U chassis. This equates to higher conduction-cooling performance and system reliability. Due to the MTC's smaller 3U form factor, it has a natural frequency significantly higher than that of larger systems. This makes MTC suitable for applications with extreme vibration and shock.

Jacob Sealander *is the manager of product line engineering for COTS subsystems at Curtiss-Wright Controls Embedded Computing – Subsystems. Jacob has been in the embedded computing industry for nine years providing mechanical designs at the card and chassis level. He holds a B.S. in Mechanical Engineering from California State University, Northridge.*

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Telecom carriers embrace AdvancedTCA/AdvancedMC platforms for emerging IP networks

By Jeff Durst

CompactPCI & AdvancedTCA

In this article Jeff outlines the role of AdvancedTCA in reducing carrier CAPital EXpenditures (CAPEX) and OPerating EXpenditures (OPEX) in the context of AdvancedMC's emergence.

Bridging the gap

AdvancedTCA systems equipped with Advanced Mezzanine Card (AdvancedMC) expansion capability provide an ideal platform for building flexible, scalable systems that bridge the gap between legacy PSTN infrastructure and emerging IP packet networks. This open framework drives equipment costs down by enabling telecom OEMs to quickly configure high availability systems using affordable, off-the-shelf hardware and software components. AdvancedTCA/AdvancedMC platforms also reduce operating costs by providing a modular, field replaceable framework with integrated system management that enables carriers to scale, manage, and service their systems with a higher degree of granularity.

AdvancedTCA defines a standard (PICMG 3.0) mechanical, electrical, communications, and management framework for building reliable, highly available, and field serviceable blades and integrating them within a rack-mountable chassis. AdvancedTCA's high-bandwidth, multiprotocol protocol (Ethernet, PCI Express, RapidIO, InfiniBand) switched fabric gives it the throughput and scalability needed to host high-speed control and data plane functions in both TDM and IP networks. A large form factor (8U) and high-power capability (200 W per blade) give AdvancedTCA the capacity needed to support complex functions and high-density configurations. One example, shown in Figure 1, is Artesyn's KatanaQp Dual-Processor AdvancedTCA blade, which is suitable for access, SS7/SIGTRAN signaling, media gateways, traffic processing, wireless base stations, and Softswitches.

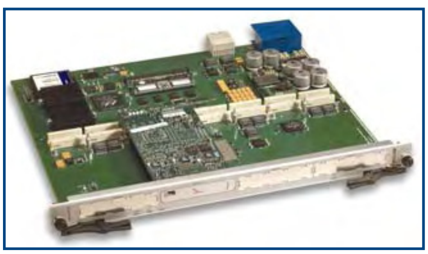


Figure 1

With its redundancy and hot swap features, AdvancedTCA reduces point failure susceptibility and enables individual blade servicing and upgrading without disrupting overall service. And its integrated IPMI system management facilities enhance availability via greater visibility into and control over blade level operation.

AdvancedMC enhances the flexibility, modularity, and scalability of the baseline AdvancedTCA fabric by extending its high-bandwidth, multi-protocol support, hot swappability, and integrated system management capabilities to individual modules. Like AdvancedTCA, AdvancedMC provides a high-bandwidth interface (up to 21 links running at 10 Gbps) with support for multiple protocols such as Ethernet, PCI Express, and RapidIO. AdvancedMC modules are also hot swappable, enabling individual AdvancedMC modules to be added or replaced in the field without taking entire blades off line. And last but not least, AdvancedMC modules provide integrated IPMI system management, which enables chassis management to monitor and control individual modules.

One of the biggest contributors to overall AdvancedTCA/AdvancedMC flexibility is its support for multiple mechanical form factors and configurations. AdvancedTCA carriers can be equipped with up to eight AdvancedMC modules, which come in four sizes:

- Half-Height Single-Width
- Half-Height Double-Width
- Full-Height Single-Width
- Full-Height Double-Width

The modules have escalating power limits of 20 W for the smallest module (Half-Height Single-Width) to 60 W for the largest module (Doublewide Full-Height). AdvancedTCA/AdvancedMC mechanical flexibility enables designers to partition for maximum scalability, upgradeability, and field serviceability. By combining generic AdvancedTCA blades with application-specific AdvancedMC modules, designers can create scalable, high-density blades dedicated to specific functions:

- Control
- Signaling
- Transcoding
- Interfacing
- Packet processing

They can also use AdvancedMC modules to combine multiple functions on a single blade and alter the mix as applications and/or system partitioning changes. Either way, this increased modularity enables TEMs to build systems that can be scaled, upgraded, provisioned, and serviced with a much finer degree of granularity, greatly reducing both CAPEX and OPEX.

AdvancedTCA/AdvancedMC reduces carrier CAPEX

Open architecture AdvancedTCA platforms reduce design time and cost by enabling TEMs to outsource system-level infrastructure and giving them instant access to mass produced, plug-and-play, off-the-shelf components. These savings are ultimately passed on to service providers in the form of reduced CAPEX.

AdvancedMC magnifies these economies of scale by enabling TEMs to build application-specific blades using generic, high-volume AdvancedMC components such as network interfaces, network processors, DSP farms, mass storage devices, and encryption/decryption engines that are reusable across multiple blades. For example, a T1 module underpinning a family of multi-channel WAN interface blades could also be used to provide a network interface for a signaling or media gateway blade. Similarly, as shown in Figure 2, an AdvancedMC-based DSP farm or network processor could be used across a slew of media gateways requiring transcoding, protocol processing, or other high-speed computing.

AdvancedTCA/AdvancedMC modularity also reduces cost by reducing the number of unique blades that TEMs have to purchase and stock. With AdvancedTCA/AdvancedMC, TEMs can stock a single generic carrier board that spans several products, along with the AdvancedMCs needed to configure that carrier for specific applications. This is not possible with traditional mezzanine architectures like PMC because PMC modules aren't field replaceable. They're typically bolted on at the factory and sold to TEMs as a single unit. Thus, the TEM has to purchase and stock a unique board for each application, regardless of the commonality that exists from one board or application to the next.

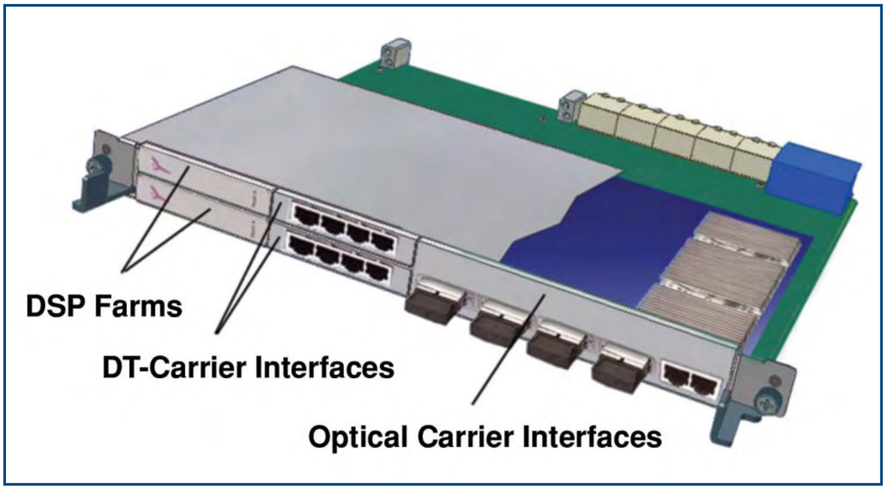


Figure 2

AdvancedTCA/AdvancedMC systems which are modular and field-replaceable are also easier to upgrade. In addition they are less expensive to scale, reducing equipment costs by enabling carriers to deploy the minimal hardware needed to service their subscriber base. Consider, for example, an AdvancedTCA based core router equipped with AdvancedMC based network processor modules, or a VoIP gateway equipped with AdvancedMC based transcoding modules. Both systems could be deployed in a minimal configuration and scaled later by adding blades (or individual AdvancedMC modules) without taking the gateway or router offline.

AdvancedTCA/AdvancedMC reduces carrier OPEX

Though open, modular AdvancedTCA/AdvancedMC platforms offer considerable CAPEX savings, what makes them most attractive to service providers are the long-term savings they offer for OPEX. In particular, AdvancedTCA/AdvancedMC systems provide a rugged, modular, fault tolerant, field replaceable framework with integrated system management that enhances reliability, availability, and serviceability, thereby reducing OPEX.

One important way that AdvancedTCA/AdvancedMC systems reduce OPEX is by reducing the impact of component failures. Because AdvancedTCA/AdvancedMC blades and modules are field replaceable, AdvancedTCA systems can tolerate failures to individual blades

and modules with minimal disruption to overall service. Consider, for example, an AdvancedTCA WAN card equipped with eight AdvancedMC modules, each providing four T1 channels. A failure in any particular T1 channel might at most take out four T1 channels (one module), versus all 32 for a monolithic blade on which the 32 channels are mounted directly to the baseboard. Similarly, failures to any single AdvancedMC module on a multichannel SIGTRAN signaling blade or DSLAM blade would only impact the signaling links or subscriber connections provided by that module.

Modular AdvancedTCA/AdvancedMC blades also reduce provisioning cost by enabling systems to be scaled and provisioned according to actual demand. Consider, again, an AdvancedTCA WAN card equipped with eight AdvancedMC cards, each providing four T1 channels. In this configuration, the T1 channels can be added and provisioned in blocks of four rather than 32. This fine granularity also reduces the cost of sparing. Regardless of the number of active channels used in the system, spare replacements (online and on-the-shelf) usually require only one or two modules, not an entire 32-channel blade.

Integrated system management reduces CAPEX and OPEX

One of the greatest contributors to overall CAPEX and OPEX savings in AdvancedTCA/AdvancedMC systems is the integrated PICMG 3.0 system management framework. Figure 3 illustrates such a framework. Based on the Intelligent Peripheral Management Interface (IPMI), the PICMG management framework reduces development costs and enhances RASM by providing active monitoring of and control over individual AdvancedTCA blades and AdvancedMC modules. This capability is especially important for high-density systems utilizing large numbers of high-performance processors, where thermal control and power management are major concerns.

IPMI utilizes an I2C based physical interface known as the Intelligent Peripheral Management Bus (IPMB) to link chassis management with board-level Field Replaceable Units (FRUs) that support IPMI. IPMI can be used to monitor physical system health characteristics such as voltages, fan speeds, temperatures, and power supply status. It can also be used for automatic event notification and remote shutdown/restart. Together, these facilities give system engineers and administrators flexible, interoperable access to a broad range of platform information.

AdvancedTCA/AdvancedMC blades transmit event information via the IPMB to a chassis management system, which makes decisions and takes the necessary system actions to ensure proper operation and report boards that need attention or servicing. The chassis management system typically records the events in a System Event Log (SEL), which enables technical personnel to look through the logs, detect trends and patterns, and determine the sequence of events that led up to a given fault condition.

IPMI based system management greatly simplifies system design by enabling TEMs to monitor, test, and diagnose systems at the blade level during the development phase. The standard management interface also gives TEMs the option of purchasing management software off the shelf. This combination reduces overall development time, which translates into lower equipment costs and CAPEX for service providers.

The most significant benefits of standardized system management become evident once the system is deployed. From an availability standpoint, IPMI makes it possible to isolate problems faster with a finer degree of granularity, thereby reducing Mean Time to Replacement (MTTR) and stocking costs.

IPMI's standard management framework also reduces OPEX by simplifying integration and maintenance. Because IPMI can be used throughout the system, service providers do not have to deploy, integrate, and master multiple custom management frameworks. The familiarity and consis-

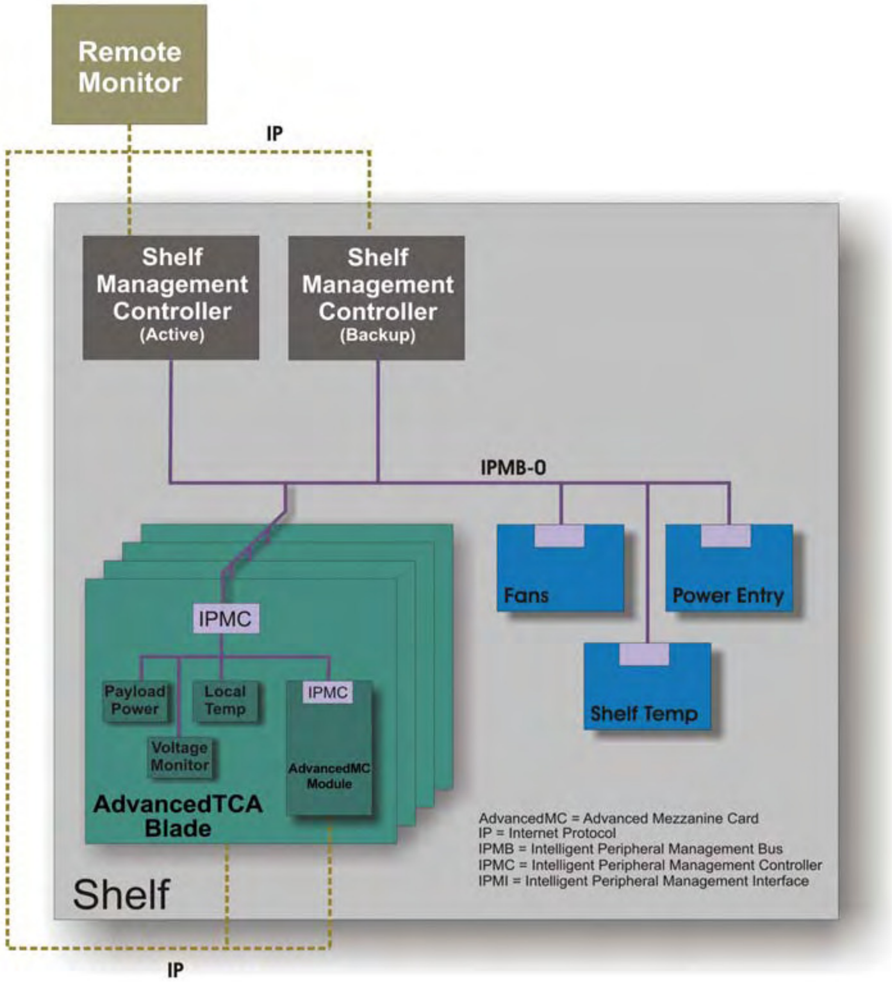
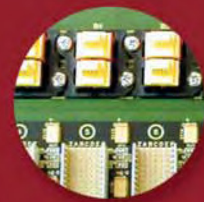


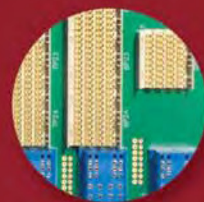
Figure 3

VME Multidrop Bus



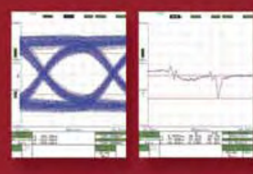
Optical/cPCI Bus

Switched Serial Fabrics



Advanced Serial Switching

Simulation/Backplane Characterization



tency of the IPMI framework also simplifies training and makes it possible for service providers to outsource the management function on a competitive basis (not tied solely to the equipment provider).

IPMI's standard management framework also simplifies upgrades and reduces the OPEX associated with adding new services. Unlike custom management solutions, IPMI enables service providers to add new services by purchasing off-the-shelf components that plug directly into the existing IPMI framework. In this scenario, the cost of powering the new blade becomes the only operational cost associated with adding new services or scaling existing ones.

Negotiated power management

Another key way that IPMI reduces service provider OPEX is by supporting negotiated power management, which helps chassis management optimize system-wide power consumption and cooling budgets in high-density systems. This system-wide capability is especially important for high-density, high-power platforms like AdvancedTCA, where the power consumed and heat generated by individual boards, though within acceptable limits, exceeds overall system budgets when viewed in the aggregate.

Consider, for example, a frame with three AdvancedTCA shelves, each populated with 16 blades. If each blade consumes its maximum 200 W, total power consumption for the rack will approach 10 kW. Even if the plant is capable of supplying this power, the frame may generate more heat than the room can accommodate, and the fans/blowers used to cool the rack may generate noise that exceeds allowable sound pressure levels.

Negotiated power management facilitates optimal power efficiency and cooling by enabling chassis management to negotiate with individual blades for power allocation prior to powering on, and then renegotiate that allocation while active. Active power negotiation:

- Increases effective power density and enhances availability by enabling shelf management to dynamically throttle back power to idle or nonessential boards
- Enhances availability by enabling shelf management to ensure continuous operation for the most important boards when total power usage and heat generation threatens the available budget
- Increases effective power density by reducing overall power consumption, which enables service providers to deploy more heavily populated systems

Conclusion

AdvancedTCA's rugged, high-performance, hot swappable fabric, together with its high-power capability, modular form factor, and integrated system management, provide a total framework for designing, deploying, and servicing telecom infrastructure systems that enhance reliability, availability, scalability, and manageability. AdvancedMC enhances these benefits by enabling service providers to deploy, scale, provision, manage, and repair their systems with a finer degree of granularity. Together, AdvancedTCA and AdvancedMC provide an ideal platform for deploying flexible systems that bridge the PSTN and emerging packet networks while minimizing both CAPEX and OPEX.

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Lead-free and waste prevention requirements in the European Union: Cleaner products at lower cost

By Hermann Strass

CompactPCI & AdvancedTCA

The term lead-free *describes a number of technical and environmental issues with the goal of removing hazardous substances and reducing the amount of waste. In Japan the transition into lead-free production (for consumer products only) is almost complete. The European Union (EU) has set more ambitious goals of reducing initially six of the most hazardous substances from consumer and professional products and reducing electronic waste significantly. This column and next month's column (visit www.compactpci-systems.com/columns/Technology_in_Europe for the complete two-part column) will include why and how this is currently done and how it will be done completely in the near future. All this is complex and time consuming, but to almost everybody's surprise, can save money for the manufacturer and the user if done correctly.*

Occasionally these EU directives are claimed to be unfair acts of industry protection. However, this is not the case, since European manufacturers suffer more than others. They have to comply with the laws. Manufacturers in countries outside the EU may choose to sell their lead-containing products in other markets. According to the Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive, there is no established production available yet in the EU. European companies do not have a time or technological advantage. Their production quantities are typically lower than in other parts of the world. Hence, the cost transition and running costs thereafter are higher in Europe than somewhere else. As mentioned, Japanese companies are already producing lead-free consumer products. So they might have an advantage when they do the same thing in the production of professional products for business use.

Legal requirements

Some of the legislation for RoHS and the directive on Waste Electrical and Electronic Equipment (WEEE) started about 25 years ago. So everybody knew it was coming. Both directives became effective on January 2, 2003. The EU is a union of sovereign states; therefore it issues directives rather than laws. These directives must be translated into the local languages and made into national laws in each country. Typically, this takes about 18 months. The main objective is harmonization of laws, regulations, and standards, in all of the member states to provide equal and fair trade, labor, and business conditions.

The RoHS (directive 2002/95/EC) specifies the maximum content of certain hazardous substance in goods produced or *placed onto the market* in the EU. The term lead-free is often used to generically describe all that is specified in the RoHS directive. Table 1 shows the current six hazardous substances and their maximum weight content.

The RoHS directive becomes effective on July 1, 2006. There are exceptions for national defense, fluorescent lamps, spare parts, and similar items. Manufacturers typically use the last two items on the list in large quantities to make flame-retardant plastic (such things as housing cable insulation) to comply with UL 94 and similar requirements.

The WEEE (directive 2002/96/EC) specifies the amount of mandatory recycling and nonhazardous disposal of waste material and return of products at their End-Of-Life (EOL). For example, private users in Germany can now return used electrical and electronic equipment free of charge, typically to municipal waste collection yards. This waste material is then recycled or disposed of properly. In the future, manufacturers or importers will have to finance this waste collection and recycling either directly or by paying a fee to those organizations that do it on their behalf. The term *green* is often used to generically describe all that is specified in the WEEE directive.

Categories of electrical and electronic equipment covered by the WEEE directive include:

- Large household appliances
- Small household appliances
- IT and telecommunications equipment
- Consumer equipment
- Lighting equipment
- Electrical and electronic tools (with the exception of large-scale stationary industrial tools)
- Toys, leisure, and sports equipment
- Medical devices (with the exception of all implanted and infected products)
- Monitoring and control instruments
- Automatic dispensers

This equipment list is also used to specify the applicability of the RoHS directive. Specific notes or exceptions reference some or all of these listed categories.

The WEEE becomes effective on August 13, 2005 when all consumers can return their electronic waste (such as mobile phones, com-

Substance	Proposed Maximum Concentration
Lead – Pb	0.1 %
Mercury – Hg	0.1 %
Cadmium – Cd	0.01 %
Hexavalent Chromium – Cr (VI)	0.1 %
Polybrominated biphenyls – PBB	0.1 %
Polybrominated diphenyl ethers – PBDE	0.1 %

Table 1

NI TestStand – Essential Software Technology for Automated Test

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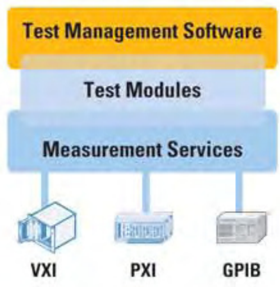
* EB300, *Electronic Business*, 2003

NI Platform for Automated Test



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puters, and CD players) free of charge to public collection points or to the original producers. Dealers may accept old product when they sell new product. The return of used cars (Directive 2000/53/EC End-of-Life Vehicles) has been regulated since July 2003.

Technical solutions

There are several dozen alloys, using tin, silver, copper, and other substances in various concentrations. It should be noted that not all have been fully qualified for long-term durability, mechanical rigidity, or neutral chemical reaction. Tin is prone to whisker growing in leaded or lead-free alloys (soldering materials), which is a serious problem. Some of the lead-free solder replacements have been found superior to lead-based solder. IBM (see report 0-0000-0000-7/03, IEEE 2003) has done substantial fundamental research to find some of these better alternatives, which show such qualities as lower inductance and improved reliability. Fujitsu-Siemens Computers (FSC) fine-tuned their solder (reflow) process for a long time. Carefully rearranging the physical position of components on a board and adjusting the speed of the board over the reflow bath is necessary to obtain best results. FSC assumes that they have a lead-time of approximately one year in comparison to competition in the mass production of consumer and business products. Equipment for lead-free reflow soldering is readily available on the world market. However, it takes a long time and extensive experience to get flawless mass production to work reliably. There is definitely no drop-in replacement for lead-based equipment or processes. The contamination of a lead-free production line with leaded components or solder residues is a very serious problem.

Most alternative soldering substances melt at higher temperatures than lead-based solder. This is a problem with certain chips or components. It is important to keep temperature and the speed of movement through the reflow trough tightly controlled, especially with reflow soldering. For example, a chip with several hundred solder balls in a Ball Grid Array (BGA) dissipates heat much faster than a diode with just two solder points. This means that the BGA might be underheated, and the diode might be overheated. Next month's column describes how one company is meeting these requirements in cost critical mass production on a big scale (with lower cost than current production), not just in isolated partial solutions in experimental set-ups.

Numerous websites cover just about every aspect of lead-free and green with focus on technical, political, or economic issues. Listed here are some starting points for your own research.

RoHS

http://europa.eu.int/eur-lex/pri/en/oj/dat/2003/l_037/l_03720030213en00190023.pdf

WEEE

http://europa.eu.int/eur-lex/pri/en/oj/dat/2003/l_037/l_03720030213en00240038.pdf
www.atsdr.cdc.gov/tfacts13.html
www.atsdr.cdc.gov/toxprofiles/phs13.html
www.cdc.gov/nceh/lead/lead.htm
www.fujitsu-siemens.com/environment
www.fujitsu-siemens.com/recycling
www.jedec.org
www.leadfree.org
www.osha.gov/SLTC/lead/index.html
www.tintechnology.biz/soldertec/soldertec.aspx

For further information, contact Hermann at:
hstrass@opensystems-publishing.com.

Eclipse Foundation extends open source to software development tools

By Curt Schwaderer

CompactPCI & AdvancedTCA

Operating systems have taken a miraculous journey over the past 30 years, from custom, internally developed kernels through commercial embedded real-time operating systems to the open source Linux world. The open source paradigm of Linux has found its way into the software development tools arena with the emergence of the Eclipse Foundation Eclipse development environment. This tool framework is written entirely in Java with the ability to plug in any number of application-specific development environments. This paradigm is also gaining significant momentum. The user and developer membership consists of more than 80 companies with far more in the general user community. A recent announcement also introduced a Spotlight on Eclipse *supplement jointly sponsored by* SD Times *and the* Eclipse Foundation. *With all this activity and momentum around this open source effort, it could be well worth your time to take a look at the organization and technology.*

Impressive growth of Eclipse

Eclipse initially went open source in November, 2001. Since that time, more than 600 commercially available plug-ins have been developed. If you browse SourceForge, you will notice more than 400 projects currently using Eclipse in one way or another. Over the past year alone, a staggering 30 million downloads of the Eclipse framework have taken place on the Eclipse Foundation servers. This number does not include the other 40 download sites around the world.

You might expect significant Linux involvement in Eclipse. You would be right. Linux providers such as Red Hat, SuSE, and TimeSys ship Eclipse C/C++ and Java development tools with their products as an alternative to the standard Linux GCC development environment.

What is Eclipse?

Eclipse is a Java based universal tools framework that has the goal of becoming the foundation for the tool building community. If the goal is realized, Eclipse will become the industry standard framework within which all tools will be built to integrate and interoperate with each other.

Currently, the Eclipse Foundation has six announced projects defined within the Eclipse development community. These projects are roughly categorized into:

- Core technology advancement of the Eclipse framework
- Technology research
- Web platforms
- Test and performance
- Business intelligence and reporting facilitation through the Eclipse tools

A Project Management Committee oversees the requirements, design, and implementation of each project. The Committee then organizes each project into the project lead, development team, and project management function.

Once the project proposal is accepted, the development life cycle goes into iterative validation and implementation phases with checkpoint reviews coming after validation and release reviews after implementation.

Who is the Eclipse Foundation?

The Eclipse Foundation founding members consist of Borland, IBM, MERANT, QNX Software Systems, Rational Software, Red Hat, SuSE, TogetherSoft, and WebGain. Since its original formation, the Eclipse Foundation has grown to more than 80 member companies.

What is the mission of the Eclipse Foundation?

In their own words, "The Eclipse Foundation is a nonprofit corporation formed to advance the creation, evolution, promotion, and support of the Eclipse Platform and to cultivate both an open source community and an ecosystem of complementary products, capabilities, and services."

Eclipse became a not-for-profit organization in January, 2004. Mike Milinkovich, executive director of the Eclipse Foundation, came aboard in May, 2004. Mike and his team focus on growing the Eclipse open source community and membership. The member-funded organization supports a staff of seven. The primary functions of the Eclipse team include:

- Supporting Eclipse projects such as handling paperwork, documentation, and IT infrastructure to support development
- Maintain Eclipse website and downloads
- Increase awareness of the Eclipse environment and its uses in various projects
- Value-add services via website
- Intellectual property due diligence

You can imagine the IT challenges involved with such a geographically distributed development team. Mike mentioned substantial work in this area to facilitate Eclipse development projects.

Funding from the Eclipse Foundation comes from *strategic user* and *strategic developer* memberships. Strategic users pay an annual fee. Strategic developers also pay an annual fee along with providing a minimum of eight developers and a commitment to lead at least one Eclipse project.

What can Eclipse do?

Eclipse provides a common foundation for creation of a robust, integrated development environment including the building, debugging, and software configuration management for software development projects. Eclipse is implemented in Java, therefore any platform with the proper Java Runtime Environment (JRE) is able to host the Eclipse development environment.

Mike also cited interesting future additions to the Eclipse framework. An Eclipse communications framework is being developed. This is a peer-to-peer communications framework to make distributed applications development easier within the Eclipse environment. He also

mentioned an *Eclipse trust framework* being led by Social Physics and *parallel development tools* project being led by Greg Watson at Los Alamos National Labs.

A brief look at Eclipse

The high-level Eclipse development architecture is shown in Figure 1. Eclipse exposes the development environment to the user through a workbench GUI environment. The workbench allows the developer to create and manage multiple projects. One or many projects defined in the workbench can be accessed and worked on simultaneously. The workbench includes a Software Widget Toolkit (SWT), which provides the tools for building graphical user interfaces and a JFace component. The JFace component facilitates the development of user interfaces and works with the SWT to allow the plug-in tool to easily provide a familiar GUI for the developer using the tool.

Users create a workspace consisting of one or many projects. The workspace is linked to a particular plug-in for the Eclipse environment, which then provides facilities such as software development, build, and debugging for the workspace. For example, one of the plug-ins available for Eclipse is a Java development environment. The specific workspace for a particular plug-in is called a perspective. The Eclipse environment allows the developer to select which perspective a particular workspace belongs to. There are perspectives for creating Java applications and C/C++ applications among others.

The Eclipse architecture provides a help framework that allows the plug-in tools developer to provide help menus for various features or tasks the tool implements. The platform runtime consists of a JRE and associated operating system running on a hardware platform like a personal computer. Finally, the Team component provides hooks for integration with a variety of software configuration management tools such as CVS.

The plug-in tools conform to the Eclipse plug-in tools interface. Plug-in developers then write an application specific plug-in using Java. Therefore, while the Eclipse environment provides an overall software development tool framework, it is the Eclipse plug-in that gives the Eclipse environment the *personality*. In other words, Eclipse provides the standard framework and user interface while the plug-in provides the actual execution of developing, building, and debugging for a specific application.

Eclipse: Not just for Java anymore

There is a common misconception that Eclipse is strictly a development tool for Java. While this capability is an available part of the environment, and Eclipse is implemented in Java, a large and far ranging group of projects use Eclipse.

Eclipse is strongly engaged in the embedded marketplace. PalmOS and Nokia use Eclipse integrated development environments as the open application development environment for their PDA and cell phone products. QNX, TimeSys, and Wind River all ship C/C++ development plug-ins for Eclipse. The Rational product line is built on Eclipse. Borland's Together Control Center and modeling tools, SAP Netweaver Studio, and IBM's Web Server Business products are also based on Eclipse.

One unique testimony to the flexibility of the Eclipse framework comes from a

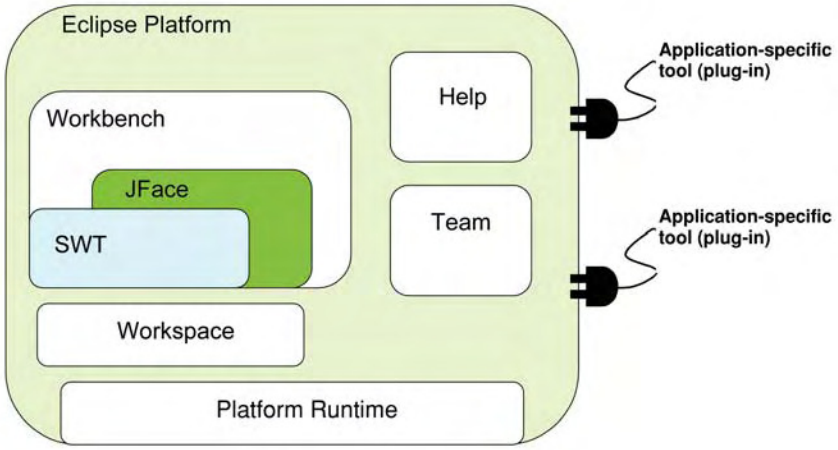

Figure 1

company called IP Fabrics. IP Fabrics has used the Eclipse framework as the development tool environment for their packet processing language runtime software environment for highly parallel network processing environments.

The myriad of available products and plug-ins based on Eclipse prove that Eclipse can be successfully incorporated into the environment not just for traditional languages, but for application-specific languages and products as well.

Always looking for contributors

Mike describes the community as a *meritocracy*, those who show interest and aptitude are rewarded with contributor status. There are no formal channels for contributing. You can begin by downloading the environment. Get involved with news groups and try things out with the Eclipse environment. If you are really ambitious, create a plug-in. If you notice problems, create bug reports and suggest fixes. Mike describes a well-formed and detailed bug report as a *small nugget of gold.* So, if you are interested in open source software and would like to get involved, the Eclipse Foundation is pleased to accommodate.

Summary

Eclipse is a large and growing community dedicated to the development of a universal tools framework upon which any *development environment* can be built. The term development environment is not just limited to C/C++ and Java projects.

Additional information on the Eclipse Foundation and Eclipse projects can be found at www.eclipse.org. This website also provides downloads for Eclipse and its associated plug-in development environments.

For further information, contact Curt by e-mail at cschwaderer@opensystems-publishing.com.

An intelligent hot-swap controller for AdvancedTCA Field Replaceable Units

By Shyam Chandra

This column examines a traditional, full-featured hot-swap controller circuit, and then suggests an intelligent hot-swap circuit that not only provides early warning to IPMC but also accepts commands from the IPMC for a controlled shutdown on the –48 V side of the power supply.

Introduction

Advanced Telecom Computing Architecture (AdvancedTCA) is a new series of industry-standard specifications for a variety of equipment such as carrier grade communications equipment, high performance blade servers, and high-speed routers. This standard is driven by hundreds of companies under the PCI Industrial Computer Manufacturers Group, and incorporates the latest trends in high-speed interconnect technologies, next generation processors, and improved reliability, manageability, and serviceability, resulting in a new blade (board) and chassis (shelf) form factor optimized for communications. Each circuit board in an AdvancedTCA shelf is called a Field Replaceable Unit (FRU).

The main reason for the development of the AdvancedTCA standard is to reduce the system cost and its time to market. Designers can leverage this standard for developing systems by simply focusing on developing their application specific hardware. This is because the AdvancedTCA standard, with its high-performance backplane, high-power distribution capability, increased reliability, and cooling meets the requirements of systems across a wide range of applications. This results in driving down the cost and increasing the availability of the AdvancedTCA base shelf manufactured by a number of vendors.

Implementation

The power distribution section of the AdvancedTCA standard is based on the use of intelligence in the power supply management. The Intelligent Platform Management Controller (IPMC) provides the intelligence to control the power on the card. There are three control elements in a power supply management circuit of an AdvancedTCA card. They are:

1. Hot-swap controller
2. IPMC
3. Secondary Power Manager (SPM)

Figure 1 shows a typical power supply arrangement in an AdvancedTCA circuit board.

The main power supply for the FRU is derived from a dual –48V power bus (Zone 1 connector). The purpose of the hot-swap controller is to limit the inrush current when the FRU is plugged into the live backplane.

An isolated power supply on the circuit board generates +12V (intermediate power supply bus) from the –48V power source. The intermediate power supply bus powers a number of non-isolated DC-DC converters required to power onboard devices. Designs often use a separate management power supply to power IPMC and SPM Integrated Circuits (ICs).

The IPMC, after power-on, communicates with the shelf manager through the Intelligent Platform Management Bus (IPMB) and provides the circuit board details. The shelf manager then issues a command to the IPMC to power the FRU. The IPMC signals the SPM to turn all the local circuit board power supplies on to power the ICs.

The SPM turns the power supplies on by following the sequencing and tracking requirements of the devices used on the FRU. Once all of the supplies are turned on and have reached their operating voltage, the SPM generates the appropriate logic signals (such as PowerGood and ResetCPU), and the FRU is said to be in normal operation mode.

Once the normal operation of the card begins, the SPM begins to monitor all the power supply voltages on the circuit board and any power supply failure is flagged to the IPMC for appropriate action. If the power supply fault is severe, the IPMC could also signal the SPM to shut the power supply off to all the circuit board devices.

IPMC intelligence serves two main purposes. First, it provides a well-controlled power-on process in an FRU, and second, it prevents fault propagation into the system. While the IPMC is able to control the power supply of the FRU on the secondary side, the hot-swap circuitry is traditionally autonomous. The IPMC gets no indication of any fault on the primary side, such as input voltage (–48V) low/high, excess current, or faulty fuses. The hot-swap controller decides the course of action for a given power supply condition and, if needed, turns the power supply off. This reduces the time available for the board to perform safe shutdown.

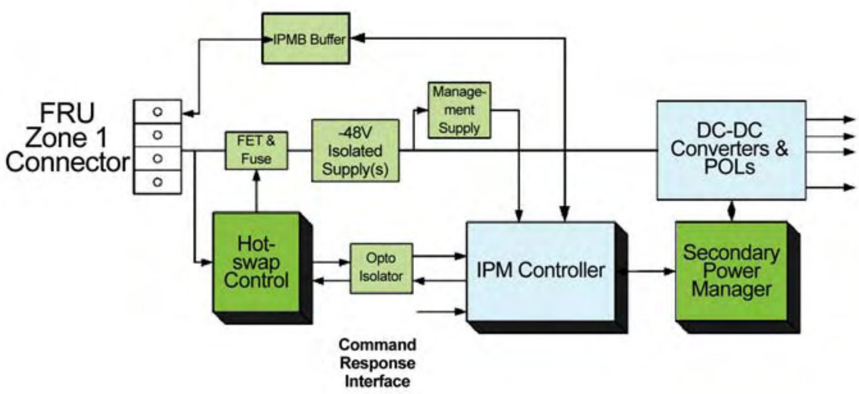

Figure 1

Consider this: If the hot-swap controller on the –48V side provides the status in real time, it increases the time available for the IPMC to perform an appropriate shutdown process. This allows time for communicating with the shelf manager, which can then flag the operator to perform such actions as checking for the fuse on that circuit board, thereby improving the manageability and serviceability of the system and resulting in a more reliable system.

Traditional hot-swap solution

The functions of a traditional full-featured hot-swap circuit in an FRU include:

Inrush current limit

When an FRU is plugged into a live chassis backplane, the onboard discharged bulk power supply capacitors draw large amounts of current from the power supply. This sudden surge in current often causes the backplane power supply voltage to dip momentarily, interrupting the operation of the circuit boards already in the chassis. The primary function of a hot-swap controller is to limit this initial current inrush. Traditionally, hot-swap controllers have used N-channel pass Field Effect Transistor (FET) devices in conjunction with current sense resistors to limit the current inrush. Additionally, this controlled the turn-on delay of the FET devices, extending the power supply connector's electrical life.

Detection of –48V Over Voltage and Under Voltage limits

AdvancedTCA explicitly describes the circuit behavior Over Voltage (OV) and Under Voltage (UV) as well as transient conditions. Designers usually resort to bulk capacitors and timing circuits in order to meet these specifications under transient conditions, since the ICs shut down the power supplies during OV and UV conditions. Hot-swap controllers just cut off the power supply to the secondary side of the circuit when the primary side power supply develops a fault. Because there is no communication between the primary and the secondary side of the power supply, power management circuitry on the secondary side has a limited time to respond to the power disconnection.

Detection of over current

Over current detection is achieved simply by monitoring the voltage across a series pass resistor in the power supply circuit, and, in the case of a fault, the power supply is cut off by turning the FET off. There is no warning generated to the secondary side.

Improving board reliability

As discussed, traditional hot-swap solutions are autonomous and do not communicate with the main board power supply controller. However, the following features, if included, provide more control over supplying power to the board and also increase the time available for responding to various types of faults. This reduces fault propagation and also prevents a forced FRU shutdown due to double faults (as in the case of a two fuse blowout fault).

Fuse detection

AdvancedTCA specifies that a fuse be placed on both the –48V and the return limbs of the power supply, resulting in the use of four fuses. Sometimes when the card is plugged into the backplane, a fuse might be open. This is because the board is designed to operate without interruption, even if one of the fuses is open. It is difficult to detect a fuse failure, and the operator will only detect failure when both fuses are open, at which time it could be too late to maintain the quality of service. If there is a mechanism in place to detect when one fuse fails, the operator could be instructed to perform maintenance before the circuit board completely fails.

Flagging UV and OV conditions to the onboard IPMC

UV indication can be used to provide an early warning to the CPU on the FRU board. This increases the time available for the CPU to safely perform the shutdown operation, including shutting down the secondary power supply following the rules of power supply sequencing.

A catastrophic OV condition can be used to shut the series pass FET off, protecting the –48V isolated power supply brick, and also providing a warning to the IPMC for safe shutdown procedure.

Flagging over current warning to the IPMC

Power supply current can be monitored to generate over current warning to the IPMC. The IPMC can then use this signal to isolate the fault, for example, a partially faulty Advanced Mezzanine Card (AdvancedMC) that is causing this over current condition, or to inform the shelf manager to increase the airflow.

If the current reaches catastrophic fault level, the series pass FET can be turned off to protect the circuit board from overheating.

Ability to isolate the card under the IPMC command

Series FETs offer a second level control for powering off a circuit board under onboard power supply fault conditions. The IPMC can also use this mechanism to completely isolate the card from the backplane and prepare for card extraction.

In the case of AdvancedTCA boards with multiple –48V isolated power supplies, IPMC could turn on the second isolated power supply brick by another series FET to meet the increased power requirement.

IPMC controlled retry power cycling

Retry power cycling is a process by which the hot-swap controller turns the series FET off, waits for the primary side to power off completely, and waits for a duration of, say, one second before turning it back on. Simulating the card extraction and reinsertion might require this, or the diagnostic system might need this to classify a fault on the board as either temporary or permanent. In addition, retry power cycling might be necessary for implementing a total carrier board reconfiguration after replacing a faulty AdvancedMC, for example. In all these cases, the power retry can replace mechanical operation, resulting in increased connector life.

Circuit description

Based on a programmable power manager, which in this case happens to be the ispPAC-POWR1208P1 (Power1208P1), an intelligent AdvancedTCA compliant hot-swap circuit is shown in Figure 2. This is a canned AdvancedTCA hot-swap power control solution. Starting from the left of the Power1208P1, two sets of the resistor divider circuits are used to monitor all four fuses (pins: Fuse_48V, Fuse_Rtn). The next portion of the circuit on the top left side of the device (VDD and GND) is the power supply to the device, which is regulated by a zener diode. Continuing on the top of the device, the next section monitors –48V for four different analog inputs with individual thresholds (V_Too_Low, V_Low, V_High, V_Too_High). Usually, the V_Low and V_High thresholds are used for generating supervisory signals to the IPMC. The V_Too_High and V_Too_Low thresholds are used for disconnecting the series FET.

The inputs I-Too_High and I_High monitor for current on the circuit board. The I_High current threshold is used to send an over current signal to the IPMC. The I_Too_High Threshold turns off Series FET, protecting the circuit board. The Brd_On signal controls the series FET enable circuit. This programmable output pin works as a switch and as the soft start mechanism to limit current inrush. The outputs on the right side of the chip (V_48_OK, No_Over_Current, Fuse_OK) are the supervisory signals to warn the IPMC of the status of the power supply. The supervisory signals are routed through opto-couplers to meet the isolation requirements between the IPMC on the secondary side and the hot-swap circuit on the primary side. The commands from the IPMC are received by the Power Manager IC, as shown at the bottom of the circuit (CMD0, CMD1), through an optocoupler.

Power supply voltage monitoring

This section monitors the –48V power supply for Over Voltage, catastrophic Over Voltage, Under Voltage, and Very

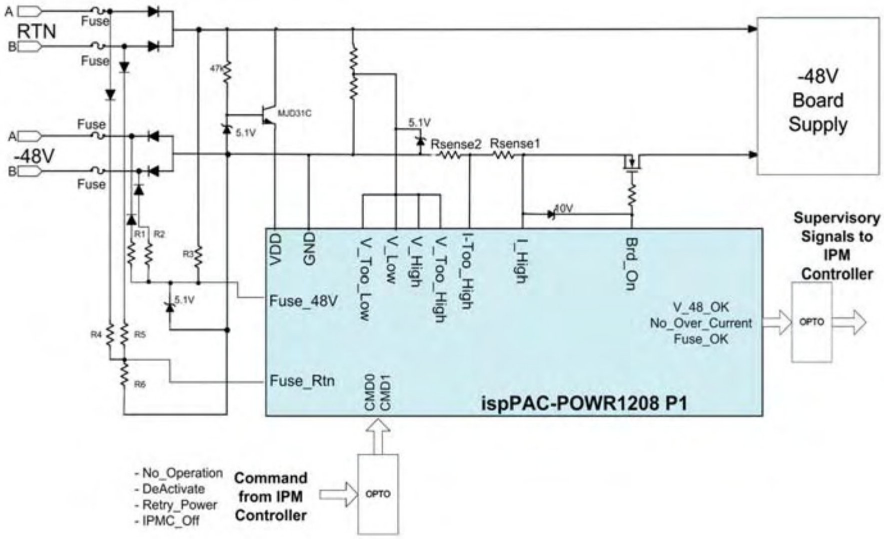

Figure 2

Low Voltage. Four analog monitoring inputs (V_Too_Low, V_Low, V_High, V_Too_High) of the Programmable Power manager device are set at different thresholds to monitor each of these conditions. When the power supply voltage is said to be in the normal operating range (more than V_Low threshold and less than V_High threshold), this is indicated by an active V_48_OK supervisory signal. When the power supply voltage is less than V_Too_Low Threshold, the Series FET is turned off after a 10 microsecond timeout and, if the voltage is greater than V_Too_High threshold, the Series FET is turned off immediately.

Fuse detection circuit

The fuse detection circuit consists of resistors R1, R2, and R3, sensing the fuses on the RTN terminals and R4, R5, and R6, sensing voltage on the –48V terminal. If either fuse fails on the RTN terminal, the voltage on the Fuse_Rtn pin drops below its threshold, resulting in the change of logic output indicating the fuse failure on either limb. Similarly, the Fuse_48V threshold detects the fuse open condition on the –48V limbs. The Fuse_OK signal deactivates when any fuse opens.

Over current protection

Over current protection is achieved by monitoring voltage drop across two resistors (Rsense1 and Rsense2) in series by separate analog monitoring inputs I_High and I_Too_High. When the current is within the normal operating limit (less than the I_High threshold) the No_Over_Current signal will be active and when the current exceeds I_Too_High threshold, the series transistor is turned off, protecting the circuit.

Inrush current limiting and Series FET control

The Brd_On is a programmable high voltage analog output signal of the Power Manager device. This output can be programmed to control the FET turn-on ramp rate, and the programmable output pin has 32 different ramp rates settings.

The Series FET device is also used for turning the power supply off for the entire circuit board. These conditions result in the Series FET being tuned off for protection:

- –48V is either too high or too low for more than 10 milliseconds.
- Current is too high.
- IPMC sends a *Deactivate* command.
- IPMC sends a *Retry_Power* Command (Series FET will be turned off until the secondary side is completely off, wait an additional one second, and turned back on).

IPMC command and supervisory signal interface

There are three supervisory signals generated by the Power1208P1. They are:

1. –48V_OK indicates that the –48V source is within the operating limits.
2. No_Over_Current indicates that the power supply current is healthy and is within limits.
3. Fuse_OK indicates that all four fuses are intact.

The IPMC generates two command bits, CMD0, CMD1:

- 00 – All power supplies are OK and the Power1208P1 need not take any action.

- 01 – Deactivate circuit board: Turn the series FET OFF.
- 10 – Retry power supply: Turn OFF the series FET, wait for all the board supplies to turn off, and continue to wait for one more second and turn the FET back on.
- 11 – IPMC is off: Indicates that all the power supplies on the secondary side are off.

Software code for the Power1208P1

Figure 3 shows the algorithm implemented using the LogiBuilder utility built into the PAC-Designer software tool. The Power1208P1 begins executing from step 0 as soon as the power supply (in this case the –48V at the backplane) to the device is turned on.

This design is compiled by the software and a JEDEC file (JEDEC is the standard that defines the structure of the file that stores the programming information for any programmable device) is generated that can be downloaded into the chip.

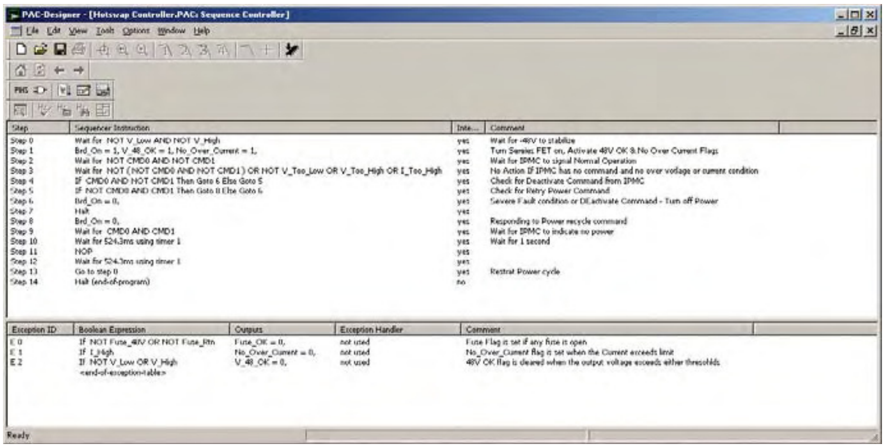

Figure 3

Conclusion

Intelligence improves board reliability

The early warning mechanism built into the hot-swap circuitry increases the time available for fault handling on the secondary side, resulting in increased functional board reliability. By incorporating the command control ability into the hot-swap circuit, the IPMC will be able to contain the problem to the circuit board with ample time to react. This increases the reliability of the circuit board even further. The device provides unprecedented convenience to the designers of AdvancedTCA hot-swap circuits.

Software based design results in flexibility

Not all circuit board requirements are identical. Because the command and supervisory warning algorithm of the hot-swap controller is implemented completely in software, it is very easy to modify the algorithm. For example, to alter the voltage thresholds monitored,

just reprogram the V_Low and V_High thresholds. If additional monitoring signals are required, just redefine the output signal equations in software.

Additional functionality that can be programmed

Addition of intelligence to the hot-swap circuitry makes additional features available that were not possible even with sophisticated, full-featured traditional hot-swap devices.

For example, it is possible to add a –48V isolated supply to power the AdvancedMCs of the circuit board with its own series pass FET, along with another command signal from the IPMC, to control this new power supply. Thus the additional –48V supply can be switched on in response to a power consumption increase grant from the AdvancedTCA shelf manager.

It is also possible to sense each fuse separately and generate a Fuse_OK signal for the A and B limbs separately, enabling the system to detect other types of faults. If the A side is online and the fuse in series with the A limb of the power supply is faulty, then the fault becomes more serious and might require immediate attention, as opposed to an open fuse on the B limb when the A side is online.

The software source mentioned in this column is available from the author upon request. To download the PAC-Designer software, visit www.latticesemi.com.

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Advanced Mezzanine Card theory of operations

By Lawson Guthrie and Mark Summers

In this second tutorial in the Advanced Mezzanine Card (AdvancedMC) series, Lawson and Mark describe the industry's next-generation mezzanine standard. They give an overview of the AdvancedMC.0 specification, including configuration options, summarizing the theory and operation of AdvancedMC usage. By providing a base-level review of configuration options, this article should help developers decide whether AdvancedMC.0 warrants further investigation. For an introduction to the AdvancedMC design goals, see Advanced Mezzanine Card Design Goals *in the November 2004 issue of* CompactPCI and AdvancedTCA Systems.

Mission-critical communications and industrial applications require hot swap capability that enables maintenance personnel to exchange field replaceable units without bringing down essential systems or processes. The front-serviceable AdvancedMC module is designed to hot swap into an AdvancedMC connector, which is seated parallel to the host carrier board. It should be noted that future revisions of the AdvancedMC specification are expected to define a standard approach for non-hot-swappable modules, which may be used to reduce costs in selected applications.

Figure 1 illustrates a Conventional Carrier with two Single-Width and one Double-Width Full-Height Modules. Note the guide rails and AdvancedMC connector on the board. The carrier is shown without the Side 1 component cover. Also shown in Figure 1, the carrier faceplate includes one or more openings through which the modules are inserted into AdvancedMC bays. Module guide rails support the insertion of the modules into the AdvancedMC connectors. The AdvancedMC bay provides mechanical support as well as electromagnetic interference shielding.

A one part, replaceable connector attached to the carrier board makes connectivity between the AdvancedMC and the carrier possible. The connector resides on the carrier board at the rear of the AdvancedMC module.

The module's I/O can be implemented through either the faceplate or the AdvancedMC connector. If the I/O is implemented through the connector, the I/O may be routed on the carrier to the backplane or to a rear transition module, which is the approach most commonly followed in AdvancedTCA systems. Note that switch/hub/routers on the carrier may be needed depending on the type of I/O routed. The AdvancedMC.0 specification defines usage requirements for single-slot AdvancedTCA carrier boards.

Module width options

All modules have the same depth of approximately 173mm. AdvancedMC supports two module width definitions, Single-Width and Double-Width:

- Single-Width Modules: The standard width for an AdvancedMC module is approximately 74mm and is referred to as a Single-Width Module. A maximum of four Single-Width (1x) Modules fit across an AdvancedTCA carrier board.
- Double-Width Modules: The AdvancedMC.0 specification also supports a Double-Width Module (2x module) that enables designs that would otherwise not fit on a single-width implementation. Its 149mm width is roughly twice that of a Single-Width Module. Double-Width Modules utilize a single AdvancedMC connector. A maximum of two Double-Width Modules can fit across an AdvancedTCA carrier board.

As Figure 1 illustrates, the AdvancedMC.0 specification permits a mixture of Single-Width and Double-Width Modules. It is important to note that while most illustrations demonstrate carrier boards fully populated with AdvancedMCs, this is not required. Some carrier designs may only support one or two Single-Width AdvancedMC modules.

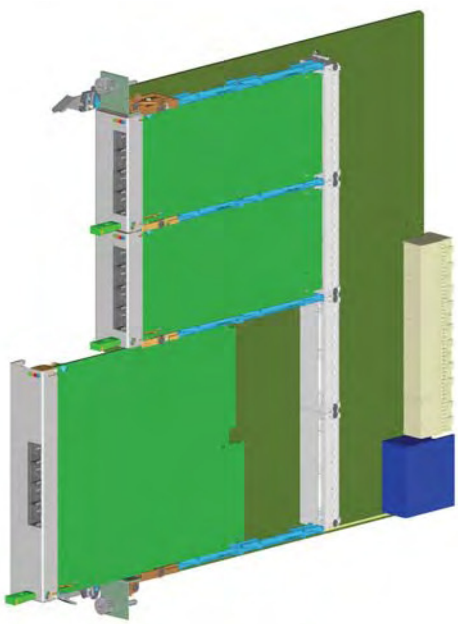

Figure 1

Module height options

AdvancedMC.0 defines two module height versions: Half-Height Modules and Full-Height Modules:

Full-Height Modules are defined to maximize the amount of component and thermal space available on component Side 1 of the AdvancedMC module. Full-Height Modules cannot be stacked.

Full-Height Modules have an optional configuration called *Extended Full-Height Modules.* The Extended Full-Height Module is required to accommodate dual-row SFPs and dual-row RJ-45s. Extended Full-Height Modules cannot be stacked. See Figure 2.

Half-Height Modules provide a reduced component height envelope on the module's component Side 1 and have a Half-Height faceplate. The term Half-Height implies that two modules equally split the maximum height available in a stacked AdvancedMC bay implementation and should not be taken literally as being half of a Full-Height Module.

Figure 3 is a Full-Height Module orientation on a Conventional Carrier. Figure 4 illustrates a stacked, Half-Height Module orientation on a Cutaway Carrier.

The module heights were set to accommodate numerous types of faceplate connectors and multiple usage models.

Table 1 provides a general summary of the different types of faceplate connectors that fit on both Half-Height and Full-Height Modules.

Table 2 presents a general assessment of a variety of AdvancedMC module usage models that would typically be expected to fit on the configurations identified.

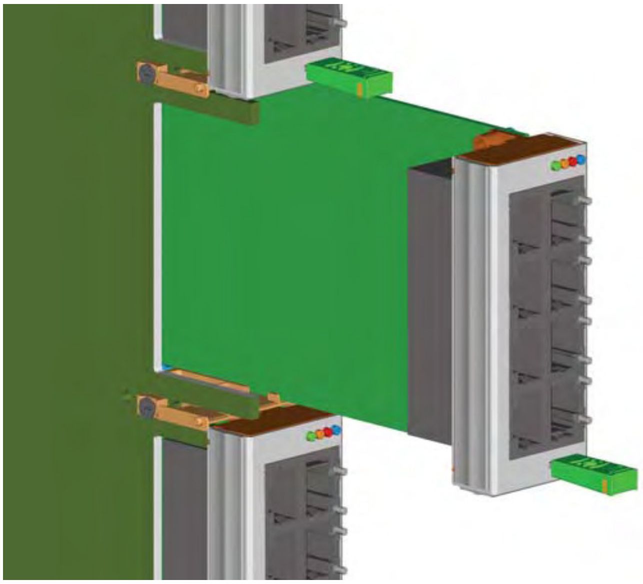

Figure 2

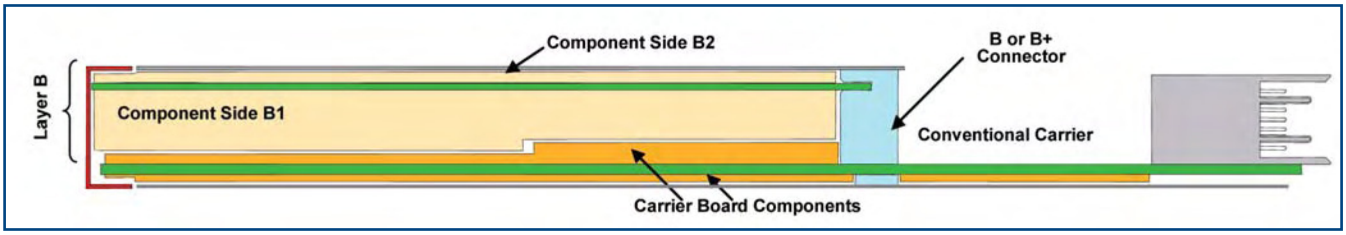

Figure 3

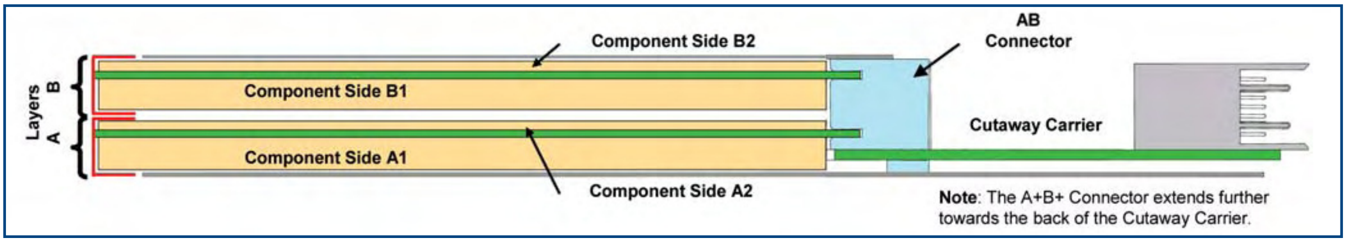

Figure 4

Connector Types	Full-Height	Extended Full-Height	Half-Height
XPAK (low profile)	Yes (1 on a 1x; 3 on a 2x)	Yes	Yes (1 on a 1x; 3 on a 2x)
XPAK2 (X2 MSA) (low profile)	Yes (1 on a 1x; 3 on a 2x)	Yes	Yes (1 on a 1x; 3 on a 2x) (Subject manufacturer specified pin length)
XENPAK	Yes (1 on a 1x; 3 on a 2x)	Yes	No
SFP (MiniGBIC)	Yes (4 max. 1x)	Yes (8 max. 1x)	Yes (4 max. 1x)
RJ-45	Yes (4 max. 1x)	Yes (8 max. 1x)	Yes (4 max. 1x)

Table 1

AdvancedMC Module Configurations	Example Functionality
Single-Width, Half-Height	Disk Drive • DSP Array • FPGA Array • Encryption Engine • T1/E1/J1 Line Cards • T3/E3 Line Cards • OC-3/12/48 Line Cards • GbE WAN Cards • 10 GbE Optical WAN Card • InfiniBand WAN Card • Memory Arrays
Single-Width, Half-Height, and Full-Height	CPU Boards • DOCSIS Cable Modem • Baseband Modem • Radio Cards
Double-Width, Half-Height, and Full-Height	NPU Boards

Table 2

Carrier types

AdvancedMC.0 supports three types of carrier board configurations:

- Conventional Carriers: The term *Conventional Carrier* refers to a carrier board without any required cutouts and allows components to be placed on the carrier below AdvancedMC modules. Conventional Carriers support both Full-Height and Half-Height Modules. Conventional Carriers also support up to four Single-Width or two Double-Width Modules across an AdvancedTCA carrier board.
- Conventional Carrier options – notched bay: In order to support Extended Full-Height Modules on a Conventional Carrier, it is necessary to notch out a portion of the carrier board for the target AdvancedMC bay (approximately 70mm of the AdvancedMC bay, starting from the faceplate). This creates the additional height needed for these modules. See Figure 2.
- Cutaway Carriers: The term *Cutaway Carrier* is derived from the carrier board below the AdvancedMC modules being cutaway to support stacked modules, as shown in Figure 5. Cutting the carrier board permits the maximum component height possible for Half-Height Modules and provides the needed space required for I/O interfaces on the faceplate. Full-Height Modules can be inserted into the upper bay of a Cutaway Carrier when the lower bay is unoccupied. Cutaway

Figure 5

Carriers can support as many as eight Single-Width, Half-Height Modules or four Double-Width, Half-Height Modules across an AdvancedTCA carrier board. A maximum stacking

of two modules is possible. Both Full-Height and Extended Full-Height Modules can be inserted into the upper bay of a Cutaway Carrier when the lower bay is unoccupied.

- Hybrid carriers: Hybrid carriers combine both Conventional and Cutaway Carrier sites on a Single-Carrier board.

Connector types

AdvancedMC.0 defines two fundamental connector types to support single-layer and stacked module implementations. These are illustrated in Figure 6.

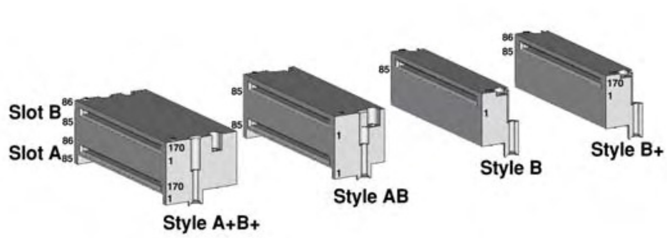

Figure 6

- B connector: The B connector is used in association with Conventional Carriers and can support a single-layer module implementation. Full-Height and Extended Full-Height Modules are supported.
- AB connector: The AB connector is used on Cutaway Carriers and supports a stacked configuration of two Half-Height Modules or a single Full-Height Module in the upper bay when the lower bay is not occupied.

AdvancedMC modules use a card-edge connection style, which features conductive traces at the edge of the module PCB. The conductive traces at the edge of the AdvancedMC act as male pins, which mate to a female connector mounted on the carrier board.

Two connector styles are specified in association with the B and AB connectors:

- Basic connector: The term *basic* is associated with AdvancedMC connectors that are equipped with conductive traces on only one side of the connector. This provides cost and real estate savings for designs that do not need a large amount of I/O connectivity. The connector for the single-sided design contains 85 pins per slot and is designated simply as either B or AB.
- Extended connector: The extended connector provides connectivity to conductive traces on both sides of the module edge. The connector for the two-sided design contains 170 pins per slot and is designated with a "+" following the connector type (for example, B+ and A+B+).

Module orientation

AdvancedMC modules on a Conventional Carrier are placed such that component side (B1) of the module faces the carrier board. The mechanical envelope is optimized for single-layer Full-Height Modules, allowing for taller components toward the front of the module. Additional components can be placed on component Side 2 (B2) of the module. Extended Full-Height Modules follow the same guidelines with the exception of the notched bay

required to support taller components towards the front portion of the module. Stacked modules are not supported on Conventional Carriers.

Figure 5 shows how Cutaway Carriers are designed to enable stacked Half-Height Modules. The stacked modules are oriented such that component Side 1 of each AdvancedMC module faces in the same direction towards where the carrier board would be. Additional components may be placed on component Side 2 (A2 or B2) of each AdvancedMC module. Cutaway Carriers may also support a single layer Full-Height or Extended Full-Height module in the B layer only.

Additional hardware for hot-swappable modules

A metal encasement above (Side 1 component cover) and below (Side 2 component cover) the AdvancedMC carrier provides additional strength and stiffness and support for AdvancedMC guide rails. These plates are required for both conventional and Cutaway Carrier configurations wherever AdvancedMC bays are located. Figures are shown without the Side 1 component cover.

Module management

AdvancedMC.0 optimizes module management for an AdvancedTCA environment. It should be noted that other platforms may require extensions to accommodate the AdvancedMC modules. An intelligent module management controller, located on every module that communicates with the intelligent platform management controller shelf controller, supports at least a defined

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minimal subset of Intelligent Platform Management Initiative (IPMI) commands. The purpose of this subset of commands is to minimize both the size and the cost of the onboard controller. Unique geographical address lines for the IPMI address of each module are also included in the AdvancedMC.0 specification. The intelligent platform management bus for IPMI 1.5 messages handles management transport.

Thermal and power

The thermal envelope's power delivery and power dissipation form key characteristics of AdvancedMC. Since higher bandwidth performance is associated with higher power, AdvancedMC expands the thermal envelope over previous mezzanines. A Single-Width Module has a 30W thermal envelope. For added flexibility, the connector can deliver 60W to the card. This allows for a Double-Width Module to be powered from a single connector and also helps to futureproof designs by anticipating improvements in thermal management technologies. In order to reduce cost and time-to-market, the AdvancedMC Side 1 height is sufficient to allow designers to reuse existing CompactPCI mezzanine solutions.

Interconnects

AdvancedMC defines a high-speed serial interface to the baseboard with 21 duplex lanes (42 differential pairs) available for data throughput. Each lane is qualified at 12.5 Gbps, which ensures longevity of the specification with advancing technology standards. These interfaces, defined through AdvancedMC.x subsidiary specifications, include PCI Express, Advanced Switching, Gigabit Ethernet, RapidIO, Serial ATA, Serial Attached SCSI, and Fibre Channel.

Summary

Telecom equipment manufacturers should take a close look at the value of AdvancedMC in their next-generation designs. You can start by downloading the AdvancedMC.0 short form specification, which is available at no charge at www.picmg.org.

In the third tutorial in this series, we will continue our preview of the AdvancedMC.0 specification by taking a closer look at AdvancedMC.0 interconnects.

__Lawson Guthrie__ is a strategic initiatives manager in Intel's Communications Infrastructure Group. He currently serves as secretary of the AdvancedMC.0 base specification and AdvancedMC.2 (GbE) subsidiary specification, as well as chair of the AdvancedMC.1 (PCI Express and Advanced Switching) subsidiary specification. Lawson has held various positions in strategic marketing over his 17-year career, focused on technology definition for network operating systems, desktop management, and telecommunications.

__Mark Summers__ is a technical marketing engineer in the Intel Embedded Architecture Division developing new markets for Intel products and technologies. As chairman of the PICMG AdvancedMC.0 subcommittee, Mark is focused on assuring a successful industry specification that will be readily adopted by industry. During his 19 years of technical experience (as employee of Motorola and Intel) spanning commercial, industrial, and military electronics markets he has been issued 20 U.S. Patents and has authored numerous technical journals.

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A COTS developer's point of view on Radio Frequency Identification

By Kevin Maier

Once in a while, there is a technology so revolutionary that it fundamentally changes the way things are done. Radio Frequency Identification (RFID) has the potential to be such a technology. Many large companies are already investing incredible sums of money at developing RFID expertise and ultimately deploying RFID products. We have seen passive RFID used in simple applications like security badges for years, and Wal-Mart has committed to a bold plan that all of their merchandise be tracked and managed by RFID in 2005[1]. The US Department of Defense (DoD) is also beginning to mandate the use of these technologies from all of its suppliers. Through the myriad of different RFID uses being investigated, there are numerous applications that could be significantly enhanced by incorporating Software Defined Radio (SDR) techniques. SDR typically requires the architectures and processing power afforded by Commercial Off-The-Shelf (COTS) products, and therefore may create a significant entry point into the RFID market for COTS vendors.

Intermodal freight containers and RFID requirements

Monitoring the location and physical integrity of intermodal cargo containers is one RFID application that can be of interest to COTS board vendors. RFID technology could be applied to this problem on a number of levels, from individual products to complete pallets, to whole containers. Additionally, monitoring may be required at any point in the supply chain:

- During actual transportation while on trucks, trains, planes, and ships
- During unloading and loading
- While cargo is located in warehouses or ports

Several different useful sensor load types could be configured with varied container configurations or requirements. A few examples:

- Refrigerator containers must be monitored on a very frequent basis. This is currently done by hand even on large seagoing ships. Integration of temperature sensors into the RFID network could save money and improve response time in the case of a refrigeration failure.
- An RFID tag attached to an intrusion detector could warn that a container had been opened, helping prevent both theft and smuggling.
- A GPS locator attached to the tag could allow constant container location monitoring with a high degree of accuracy. A constantly monitored GPS sensor would also prevent theft by ensuring that materiel is delivered to its intended destination. Additionally, there could be immediate notification if cargo shifts at sea or is in danger of going overboard. Adding manifest information to an RFID number, or even loading it into the tag itself, makes calculating the complete manifest for a ship a matter of seconds.

In light of these demanding requirements, it is useful to take a quick look at the different types of RFID that might be applicable.

Active and passive RFID

At a high level, there are two main types of RFID: active and passive. Each type requires two main categories of equipment: interrogators, sometimes called readers, and tags.

Passive RFID systems use the energy in a received signal to transmit the tag ID back to the interrogator. Typically this occurs over a very short transmission distance, uses extremely simple waveforms, moves small amounts of data, and as a result has very limited security features. Fully passive RFID systems, due to their lack of battery power, have very short ranges on the order of one meter. In our example, individual products and perhaps even complete pallets would likely use passive RFID techniques.

In both semi-active and fully active RFID systems, the interrogator sends out intermittent signals that prompt a tag to reply with data. Fully active systems feature tags that are capable of sending out query messages to the interrogator. Active RFID systems use a power source, usually a battery, in the tag to transmit when prompted by the interrogator or through an internal program. Using a power source allows longer transmission distance, greater amounts of data to be transferred, and the use of more complex waveforms. Active tags typically have a greater data storage capacity, making them useful for storing both data updates received in real time and data stored on a permanent basis, such as tag operational data. Both subtypes of RFID (active and passive) are gaining wider adoption in the commercial world and have a multitude of different applications.

Most likely, active tags developed for intermodal freight tracking and management will be engineered to the point that they are essentially Application-Specific Integrated Circuits (ASICs) due to economies of scale. A fleet of shipping containers could well require millions of tags based on the volume of cargo they transport, which would easily justify ASIC development costs. However, an advanced active interrogator can bear a striking similarity to a wireless radio/modem in terms of requirements, capabilities, and solution architecture. Interrogators are not as constrained by power, cost, or form factor as tags, and potentially require the high processing densities offered in typical COTS processing boards. By leveraging off existing technologies, development and production of active RFID interroga-

tors may be a more attractive technology to COTS board vendors.

Software defined active RFID

Although our example application follows the typical RFID model of active interrogation, there are several advantages that an interrogator based on SDR technology might bring to the table. Users can reprogram SDR modems, essentially on the fly, to utilize new or different waveforms. This gives SDR modems a key advantage in contrast to many other *stovepipe* modems that are limited to using their originally programmed waveforms. For example, dual/tri/quad band cell phones can communicate over multiple preprogrammed frequency bands and determine which band is currently available. However, they cannot accept reprogramming that would allow them to use an entirely different waveform. This capability to accept reprogramming for new waveforms would be possible with a software defined communications device.

Given this advantage of a software defined modem architecture, we can see that an active RFID interrogator product could be developed to be virtually unconstrained in the types of active tags that it could read. Merely changing the software load of such an interrogator could change the entire behavior of the system. This could also be a great benefit to ports of call, potentially reducing their infrastructure costs while increasing their quality of information. A port or warehouse could invest in a single type of RFID reader that could read multiple different tag standards at the same time, or even cycle through a library of RFID waveforms to determine the correct one when a new ship comes in for loading/unloading.

A further advantage of the software defined RFID architecture, especially in a military environment, is advanced information security. Programming could enable a tag or reader to automatically switch waveforms in the presence of jamming or spoofing attempts. Or a tag could respond differently to information requests on different waveforms; a base waveform could be used for general sensor information where a higher complexity waveform, operating at the same time, could be used for detailed bill-of-lading information.

An example architecture

A software defined RFID interrogator is essentially a Software Defined Radio, and may or may not support some of the advanced features of SDRs, depending on the system's operational requirements. A basic single channel SDR modem, as shown in Figure 1, consists of:

- The RF front-end, antenna, and analog up/down conversion if necessary
- The A/D and D/A converters
- High rate processing, typically in an FPGA
- Lower rate processing, typically in a DSP or General Purpose Processor (GPP)
- A waveform setup and control processor, typically a GPP
- A baseband transport, often 10/100/1000Base-T Ethernet

In military systems, the baseband information at this point would still be encrypted and would be transferred to the INFOSEC subsystem and on to red-side processing.

By organizing the radio processing in this manner, it becomes quite easy to change out parts of the processing to allow for different waveforms. Two caveats exist, though. All waveforms targeted by this platform must be able to use the same rate of digital conversion on the front-end, and the overall data rate cannot exceed the rates available on the platform.

Additionally, a platform vendor can provide another great advantage to waveform portability: a common operating environment inside all of the processing elements (FPGA, DSP, and GPP). By creating a common environment inside processing elements, waveforms only need to be developed once. Technology insertion becomes easy for platform vendors as newer, faster, and more efficient/cheaper processors can be substituted for older/slower processors while allowing waveforms to be ported by merely recompiling (in the best case). This also enables a waveform development platform to differ from the deployment platform, allowing a smooth transition of technologies without disrupting fielded systems.

One potential standard operating environment that is in use in military radios is the Software Communications Architecture (SCA), currently at revision 3.0. Using CORBA as an underlying middleware transport, the SCA defines a complete software radio architecture for military radios and has been designed from the ground up to enable technology insertion and waveform portability. For "guaranteed" waveform portability, a developer must use only the SCA and POSIX commands in the GPP operating environment. Figure 2 shows a software stack designed for waveform portability. The SCA is currently undergoing revision to add on a specialized hardware supplement that will extend waveform portability into the DSP and FPGA, not just the GPP as is currently specified.

A real world implementation

Oak Ridge National Laboratory (ORNL) is currently developing a suite of multipurpose software defined RFID interrogators for multiple programs addressing:

- Military logistics
- Homeland security
- Commercial transportation applications

The readers will track military assets in both hostile and non-hostile environments and monitor intermodal cargo containers.

ORNL is building their technology by beginning with developing waveforms and capabilities on an existing COTS Software Defined Radio prototyping system, Spectrum Signal Processing's *flex*Comm™ SDR-3000 (Figure 3). The SDR-3000 platform provides a complete multichannel SCA-enabled modem development environment and contains four instances of the single channel architecture shown in Figure 1. The active RFID interrogators will incorporate the SCA

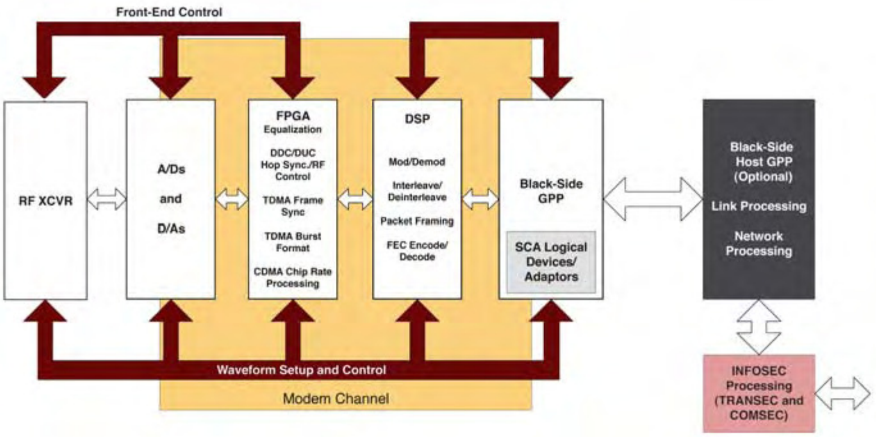

Figure 1

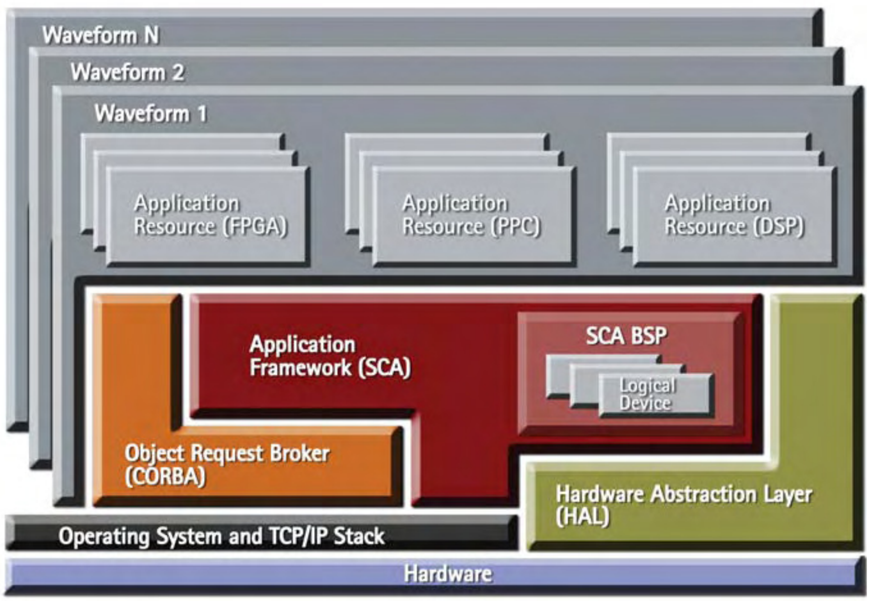

Figure 2

Figure 3

to allow them to interoperate with Joint Tactical Radio System (JTRS) communications devices. The readers will support multiwaveform operation including the support of complex waveforms designed to optimize available frequency spectrum use and prevent the jamming and spoofing of security-sensitive RFID signals. By adopting a platform selected by the US Department of Defense as a JTRS representative hardware set, ORNL can significantly reduce development time and risk. These benefits can also carry over to deployment, depending on the similarity of the software defined modem architecture as well as on the completeness of the SCA environment on the deployment platform.

Conclusion

Radio frequency identification technology can fundamentally change the nature of asset tracking. With active RFID systems, one can track richer information on more items at a greater distance with increased security. Enhancing active RFID with SDR technology and common operating environments can ease technology insertion and provide configuration options unavailable with stovepipe RFID reader architectures. Similarities between RFID and military radio modem technology can allow COTS vendors to contribute economically to the actualization of this exciting emerging technology.

Reference

[1] Feder, Barnaby, J. NY Times December 27, 2004, *Despite Wal-Mart's Edict, Radio Tags Will Take Time*

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Achieving data integrity with data security from remote locations

By Steve Rogers

As enterprises are expanding their storage infrastructure to achieve greater availability, integrity, and economies, their sensitive business critical data is being exposed to unnecessary risks and exposure due to some storage processes. Steve notes in this article that proper attention to the security issues of storage networking is long overdue and introduces new technologies for managing and backing up remote data.

Introduction

When enterprises expand into remote locations, effective data management and security become more complex. At the same time, data backup becomes a major issue as a lack of processes and adequate technology to manage and safeguard it increase risk. According to IDC, 60 percent of critical corporate data resides on remote servers, user desktops, and laptops instead of in corporate data centers. IDC also found that only 18 percent of companies believe they have adequate protection for it.

Today, new technologies for managing and backing up remote data are emerging. Because these solutions are complex, a thorough understanding of all the elements of remote data management is essential to ensure that the system you select will be able to deal with all the required elements.

Understanding the challenges of remote data

Although IT administrators in companies with remote offices spend significant time managing backup, data management, and data transfer requirements for those offices, critical processes such as backups may not be adequately covered. Often, central IT staff must rely on nontechnical staff in remote locations to change backup tapes, initiate processes, and take other actions they are neither trained nor compensated to perform. As a result, companies report as much as 60 percent of their remote backup procedures may fail on a nightly basis.

When problems do occur, recovery is tedious and takes days, assuming the data was adequately backed up. Central IT personnel may need to receive tapes from the remote site, catalog the volume and search for the files needed, and then reship the files for restore.

Online alternatives such as disk-based backup for local archiving can improve backup and speed recovery at the local site. However, these implementations can be problematic when multiple sites are involved.

Key considerations for managing remote data

Selecting the most effective remote data management tool requires understanding of several functional, environmental, and technology factors that don't come into play in a data center.

Central policy based control

Efficient control of remote data requires setting a central rule once and implementing it throughout the enterprise, rather than managing activities individually at different sites with multiple separate platform-specific policies and tools. Avoid products that claim *central control* capability yet require a unique connection to each remote node to set policy. This eats up hours of administration time during initial setup and each time a business requirement changes. The most efficient technologies provide a *set it and forget it* approach that automates policy communication to the remote node(s) and provide integrated notification if something does not proceed according to policy.

WAN network bandwidth utilization

Available bandwidth, as well as tolerance to a range of varying network conditions, must be considered. Remote locations frequently have varying bandwidth availability that needs to be shared among multiple applications and users. For this reason, remote data management and movement solutions should have features that enable efficient use of available bandwidth such as:

- Byte-level differential data transfer
- Bandwidth throttling
- Multi-streaming
- Compression

Having a fairly *skinny* network pipe can be a critical issue. To put this in perspective:

- With a 384 Kb network pipe, passing 1 GB of data would take six hours and two minutes.
- With a 1.5 Mb T1 network pipe, passing 1 GB of data would take one hour and 33 minutes.

Understanding the rate of data change between backup periods is also key. The rate of change in a *fairly busy* remote office typically ranges from three percent to five percent per day.

> Best-case scenario: 500 MB daily x 5% = 25 MB/day *very do-able with either network pipe.*
>
> Worst case scenario: 50 GB daily x 5% = 2.5 GB/day *do-able with a T1 (approximately three hours)* but not with a 384 Kb network pipe.
>
> *Note: Both of these scenarios vary greatly with compression, encryption, byte-level changes only, and bandwidth throttling levels. Enterprises should ensure that if bandwidth is an issue, their solution comes standard with these features.*

In addition to data rates, the amount of network overhead (or information) needed is also an important consideration (with less being better). Finally, since

some remote connections will likely be impaired during some processes, the ability to restart at the point of failure is critical, as is the ability to reroute information flow to alternate networks.

Security and data integrity
Data security is always a major concern in networks because all networks are susceptible to intrusion. Therefore, the solution should employ certificate authentication. This is particularly important in remote locations with fewer IT controls. Any remote data solution should, at a minimum, authenticate all sending and receiving nodes prior to any data transfer and preferably provide secure encryption of the data during transmission. Encryption levels of at least 64-bit, and preferably 128-bit, should be used for the more sensitive information. The solution should allow users to choose the level of security they wish by job in order to maximize performance. Moreover, it should utilize a single firewall port and minimize firewall rules. The ability to ensure that data is received with 100 percent integrity is also an important consideration. Any backup method should backup the data along with its security attributes so security access can be restored along with the data.

Remote process automation and application interfacing
To minimize or eliminate the need for manual effort at remote locations, the management solution must be able to automate processes and interface with remote applications to access data. For example, when backing up applications like Exchange or SQL Server, it is preferable to use native backup routines. Therefore, the remote data solution must be able to integrate with the application and invoke the native backup package as part of the backup process. The remote management solution should automate these as part of the overall remote backup process.

Heterogeneous system support
A company with multiple remote locations will commonly have a variety of computing platforms and applications at those locations requiring a solution to function within a heterogeneous environment. While this seems simplistic, many products today only work within homogeneous environments.

Point-in-time vs. continuous replication
Continuous replication products continuously monitor a file system, capture changes as they happen, and either replicate them immediately or cache the information for bulk transfer at a later time. While these products are ideal for continuous replication between small numbers of systems for business continuity purposes, they are not ideal for periodic operations such as backup and archiving. Point-in-time replication products are more appropriate and are far more network efficient for periodic processes such as backup and archive.

The case for archiving
An often-overlooked but critical component of remote data management and protection is archiving. Few users have the time or interest to clean out files, so e-mails and other files build up and contribute to the huge volume of data growing in remote storage. When asked, users cite the single biggest reason for backup failure is that the quantity of data was too large to be backed up within their backup window.

Most user files and e-mail data are seldom re-opened after the first three days of creation or receipt. If a file hasn't been accessed in 90 days, there's an over 90 percent probability that it will never be

opened. Since users can't predict what data they will need, they hold onto all of it.

The cost-effective solution is to assess the data, then move unused or least recently used data to lower-cost secondary storage (archive) with reasonably easy retrieval capabilities, for long-term retention. Once done, the frequency with which this data gets backed up is dramatically reduced or possibly eliminated altogether.

Another factor driving the need for archiving is federal document regulations such as SEC Rule 17a-4 that require many companies to retain all communication and documentation for specific time periods. For a distributed enterprise with many remote offices, ensuring compliance to these regulations can be an additional challenge.

These costs and legal requirements are compelling companies to ensure that employee messages and specific file types are archived or moved to lower cost, longer term media. Similar to remote backup, data integrity is essential to any archival solution.

Gaining acceptance as the most viable way to archive older data is consolidated archiving. With this method, enterprises move older or unused data automatically from remote disks to a central repository, often consisting of lower-cost SATA disks, while leaving pointers or *shortcuts* for access capability for the remote user.

Central policy approach to managing remote data

Relying on individual backups and separate point processes for each remote site requires local staffing, so a more effective enterprise approach is to allow central IT staff to control remote data management and backup. This requires understanding the changing properties and characteristics of remote data. Solutions should be able to:

- Set policies pertaining to the data.
- Automate processes to execute those policies on remote servers.
- Move data between remote or *edge* servers and central or *core* systems.

In this model, individual remote backup and archive processes at the remote sites are replaced with a consolidated process that moves remote data to a hub site for backup or archive. This requires moving the pertinent data over the available networks in an efficient, secure, timely fashion, and therefore requires technology that can deal with the many issues associated with controlling and moving data among many sites and network connections.

Centrally controlled, automated processes have been shown to decrease backup costs by as much as 75 percent by eliminating tapes, tape drives, offsite tape storage, and redundant staffing efforts at each location.

Combining disk-to-disk, backup with remote replication

Disk-to-disk consolidated backup is gaining popularity because of rapidly falling disk storage costs, more ready access to data for restore purposes, and the physical limitations of tape and unreliable tape storage programs.

Implemented in a best practices model, disk-to-disk backup for remote data involves moving the data to be backed up to a remote location to enable recovery from a site disaster event (such as fire or flood). For any business with multiple remote locations, consolidating these backups enhances data security as well as operational and cost efficiencies. The two primary steps to a Consolidated Backup strategy are:

1. Moving differential data to a central disk
2. Consolidating backup images

The common thread to both is central control, automation, and the elimination of individual tapes, tape drives, and off-site tape storage processes at each site.

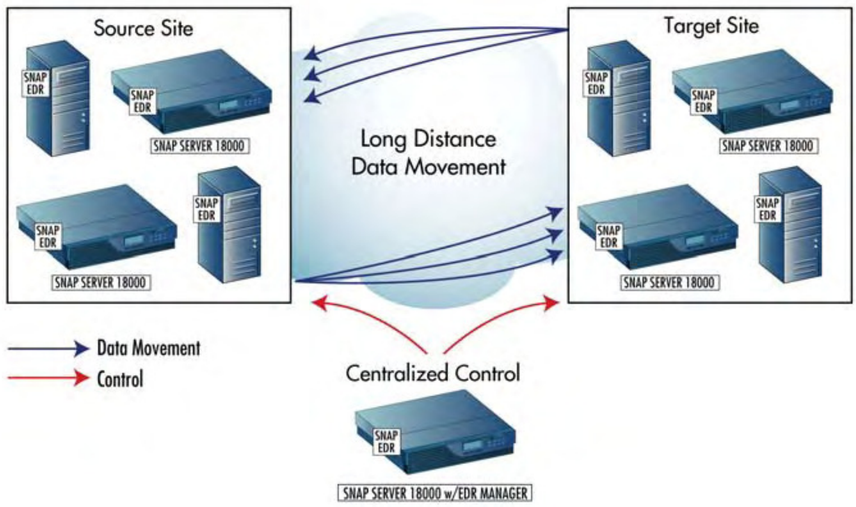

Figure 1

Figure 1 shows the first, more common approach to Consolidated Backup. With this approach, data at remote sites is periodically analyzed to determine differential data (data that has changed) since the last backup process. Companies using this method then move a copy of this differential data to a central site for disk storage. Some technologies have the ability to discern just the byte-level modifications of files to minimize the amount of data needing to be transferred. Data can be stored as incremental packets of data or reconstructed on the central site to provide full, up-to-date copies of remote files. This latter alternative has the advantage of providing instant access to individual files in the case that a remote file is accidentally deleted.

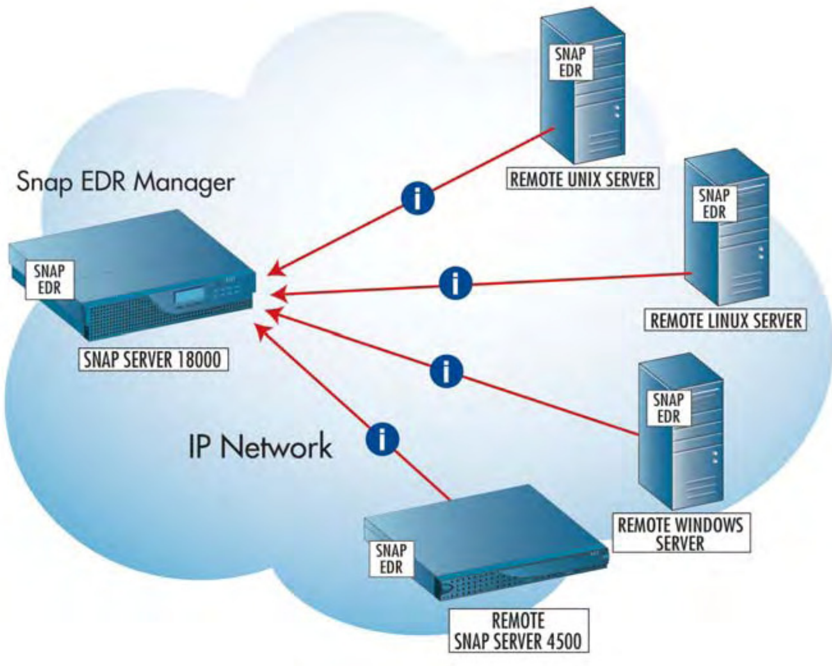

Figure 2

In the second approach (Figure 2), backups are run on remote servers with the output stored to the local disk. The resulting backup image is then transferred to disk at the remote site. This works well for applications that have native backup or snapshot features that can be utilized in the Consolidated Backup process.

These approaches can also be used together. For example, backing up user files may be best performed with differential data transfer, while backing up Exchange data may be best performed using the Consolidated Backup image approach.

In both approaches, the backup data on disk at the core location can be further sent to tape if desired. Companies often choose to keep one or two days of backup data on disk for instantaneous access, with older data written to tape.

Consolidated Archive

Consolidated Archive involves identifying remote data that meets corporate archival policy and then moving that data from remote systems and archiving it to a central disk. The corporation's archival policy determines what data should be archived when, and often includes last date accessed, type of file, content, location, ownership, and size of file, among other factors. A consolidated archival process has many benefits. The amount of data can be reduced, which reduces the required backup window. The remote disk can be optimized for better performance and cost, and compliance to data retention policies and regulations can be ensured.

An essential part of Consolidated Archive is some mechanism for retrieval of data

from the archive by end users, preferably without the involvement of IT.

Central policy based consolidated processes such as Consolidated Backup and Archive provide an approach to managing data at remote offices that can significantly lower costs, eliminate risk, improve data consistency, and also ensure better compliance to corporate backup and retention policies. It is an approach that all businesses with remote offices should actively consider.

Summary

As enterprises become more complex and geographically distributed, so does the task of managing and securing data. A full understanding of the elements discussed earlier is essential to enable data storage professionals to select the best product for automating the logistics of effectively managing remote data.

Look for high performance data replication and management solutions that are WAN network-optimized, such as the Snap Enterprise Data Replicator solution (Snap EDR) recently introduced by Adaptec, to enable easy, cost-effective data movement, protection, and reporting throughout a distributed enterprise.

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HA designers think outside the box

By Paul N. Leroux

Studies indicate that software-related issues, including software errors and software upgrades, account for most service outages. Paul makes the case in this article that achieving HA must, as a result, start with the software foundation on which all HA applications are built: the OS.

A systems problem

There's no shortage of High Availability (HA) products on the market, many of them promising 5-nines or greater reliability. Question is, can HA really come out of a box?

The numbers tell the story. To achieve 99.999% reliability, an application can experience no more than 5.25 minutes of downtime a year – it doesn't matter how many software faults, power outages, hardware failures, operator errors, or other gremlins pop up. In fact, if an application were removed from service for just one hour a year for software upgrades, it would achieve a miserable 4-nines availability rating: 99.99 percent.

With numbers like these, it soon becomes obvious that HA is, in fact, a systems problem. The entire solution, including the Operating System (OS), hardware platform, and application code, must be designed with HA in mind. For instance, how does the OS handle driver faults, a common cause of system crashes? Can the OS immediately restart the rogue driver without a system reset? Or must the entire system be rebooted?

Even physical security comes into play. If a system is located where unauthorized personnel can physically tamper with it, maliciously or otherwise, it can't realistically qualify as an HA system. HA can also extend to operator training and human factors engineering. If a system failure requires manual intervention (for instance, replacing a faulty CPU card), operators must learn how to solve the problem promptly, and the system itself must be designed to make the repair job easy.

Even if an out-of-the-box solution could provide HA, it might not be the kind of availability the user requires. To understand, consider that an HA design does more than simply try to prevent failures. It must also recover from any error or system upgrade within a very brief (and hopefully predictable) time frame. This can be expressed in a simple formula (see Formula 1) where *A* is availability, *MTTF* is Mean Time to Failure (average length of time the system will operate before failing), and *MTTR* is Mean Time to Repair (average time it takes for the system to return to service after any component fails or is upgraded):

$$A = MTTF \div (MTTR + MTTF)$$

Formula 1

From this, we can deduce that system A could fail more often than system B, yet both systems could have the same availability rating, provided that A had a shorter MTTR. But would system A be more of a nuisance or a danger to users? It all depends on the application, of course. But, clearly, to achieve a meaningful degree of HA, the systems designer must first understand what kind of service (and service outages) users prefer, then design the system accordingly.

Nor is an HA rating meaningful until you look at how partial service outages are handled. For instance, say the performance of a network degrades to the point where transmission quality becomes unacceptable. The system may be operational, but is it truly available to the customer? Not really. Actually, this brings up another point: network management – along with technologies such as redundant or load balancing network links – can form yet another part of the overall HA equation.

Software: the biggest challenge

If hardware were the only consideration, most systems designers could achieve HA by adhering to a few time-tested principles:

- Prefer circuitry to mechanics.
- Avoid fans by selecting cool-running devices.
- Choose components designed for easy repair or replacement.
- Look for rugged construction.

In fact, a rich variety of "HA" hardware platforms that embody these principles can be purchased off the shelf. Many of them are based on CompactPCI or AdvancedTCA, both of which support a number of HA-related features, such as hardware hot swap for dynamically replacing obsolete or faulty components.

The biggest problem, however, is software. Studies indicate that software-related issues, including software errors and software upgrades, account for most service outages. Achieving HA must, as a result, start with the software foundation on which all HA applications are built: the OS.

Driver, heal thyself

To appreciate the role of the OS, consider the principle of fault isolation and recovery – a key concept in HA. According to this principle, a fault in any software or hardware component must not throw other components into error states; otherwise, system-wide failure may occur. Moreover, the faulty component must be quickly replaced or restarted, while the rest of the system continues to run.

This requirement poses an inherent problem for conventional RTOSs, since they typically run most or all software components in the same memory address space as the OS kernel. In this architecture, a corrupt pointer in even a trivial component can overwrite kernel memory and thereby crash the entire system. So much for fault isolation.

Some RTOSs attempt to address the problem by running applications in separate, memory-protected address spaces. If an application attempts a memory violation, the MMU will catch the fault and alert

the OS, which can then take appropriate action (for example, slay the offending process, then restart it). Unfortunately, these OSs still bind drivers, protocol stacks, file systems, and other system services to the kernel, which means that any of these components can induce a kernel fault. In other words, each driver or protocol stack remains a *Single Point of Failure* (SPOF) – a component whose failure can render the entire system unusable.

Other OS architectures, such as the microkernel architecture used in the QNX Neutrino RTOS, go one step further and allow every system service to run in its own MMU-protected address space. Faulty drivers and protocol stacks no longer act as SPOFs, but instead can be stopped (and automatically restarted) before they cause other services to fail. See Figure 1.

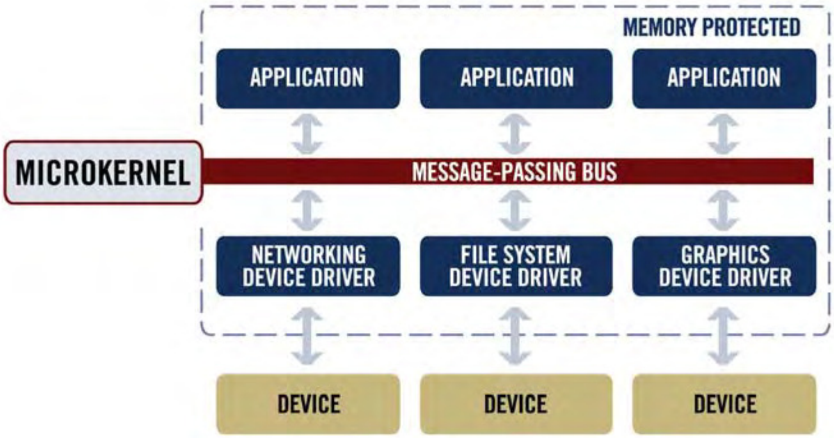


Figure 1

Fixing it before it breaks

This last type of OS architecture enables another key requirement of HA: the ability to repair software errors before they have a chance to recur. For instance, if a driver attempts to write to memory allocated to another process, the MMU will notify the OS, which can then pass control to a program called a software watchdog (a.k.a. process monitor). The watchdog can then do two things:

1. Restart the driver and, if required, any related processes.
2. Generate a process dump file that can be analyzed with source-level debugging tools.

Using this dump file, the software developer can immediately identify the source line that caused the fault and inspect diagnostic information such as the contents of data items and a history of function calls. With this information in hand, the developer can quickly engineer a fix that can be uploaded to other units in the field, often before they experience similar failures. See Figure 2.

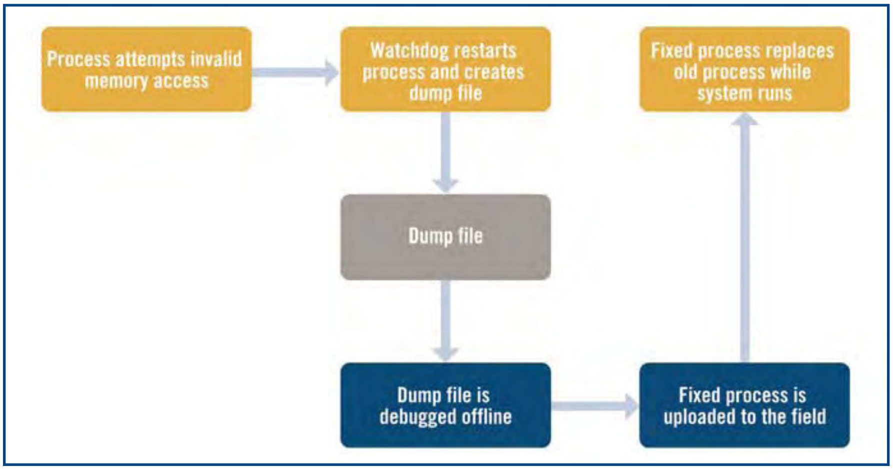


Figure 2

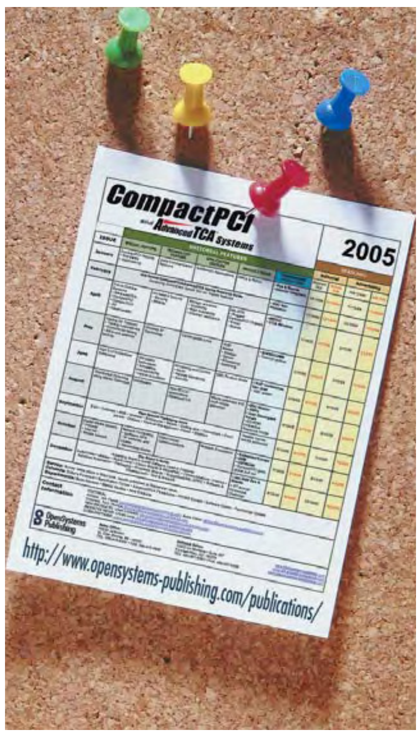
Better still, a software watchdog can be used to monitor system events that are invisible to a conventional hardware watchdog. For example, a hardware watchdog can ensure that a driver is servicing the hardware, but may have a hard time detecting whether other programs are talking to that driver correctly. A software watchdog can cover this hole and take action before the driver itself shows any problems.

A software watchdog may offer a number of other features, such as:

- Heartbeating – Allows the watchdog to monitor the progress of any software component and to detect problems before they escalate to an unrecoverable state.
- Resilience to internal failures – If the watchdog stops abnormally for any reason, it should be able to immediately reconstruct its own state.
- Watchdog API – For telling the watchdog what actions it should take should an error condition occur.

Making the (up)grade

A higher-end networking element or industrial control system may have to be upgraded with new software several times a year. In most such systems, downtime isn't an option: the system must continue



to provide service while the upgrades take place. As with other HA software issues, the responsibility for enabling such upgrades falls squarely on the OS.

When it comes to upgrading application-level code, most modern OSs have little problem. In fact, some OSs even allow new system services, such as drivers and protocol stacks, to be dynamically attached to the kernel. However, because these services then run in kernel space, they can't easily be stopped, removed, and replaced with new versions. Upgrading them becomes difficult, if not impossible, unless the system is removed from service and rebooted.

To address these problems, an OS should, at a minimum, allow drivers and other services to be dynamically unloaded. However in many cases a driver may have to be upgraded without interrupting the service that the driver itself provides. As a result, the OS should allow a new version of the driver to start while the old version is still running, and then allow the new version to gracefully take over the existing driver's duties. Once the transition is complete, the OS could terminate the old driver and recover whatever resources it was using.

A matter of design

Designing for HA requires a split personality. The systems designer must first ensure that faults – in both hardware and software – happen as rarely as possible. But the designer must also assume that faults will occur and take precautions to ensure that the system recovers quickly.

The question is: which precautions are necessary? To answer that, the designer must first determine which services in a system actually require HA and what degree of HA each of those services needs. Once that has been decided, the designer can begin to identify any potential SPOF, that is, any component – be it a CPU, networking card, power supply, or software module – whose failure can impede or stop delivery of the service.

Redundant choices

Having identified potential SPOFs, the designer can decide on what kind of redundancy, if any, is required. There are two basic choices: *N* redundancy (2*N*, 3*N*,...) where every component is duplicated, or *N*+1 redundancy where only selected components have a backup. A 2*N* design can often provide faster switchover times than an *N*+1 design but can also be much more expensive if, for instance, the system has a large number of I/O connections (as in a switch). In that case, a single spare connection could serve as the standby for several active connections.

Redundancy may be extended to any resource, including, for example, network

links. The redundant links could act as standbys or provide load balancing for greater throughput. See Figure 3.

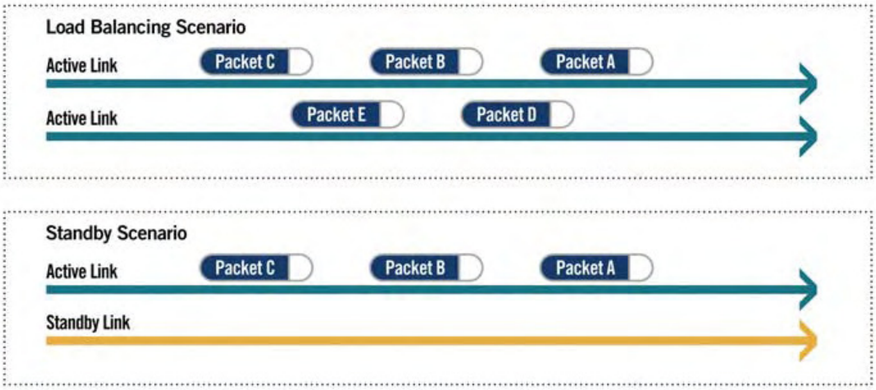


Figure 3

Besides deciding on the form of redundancy, the systems designer must establish what restart model the redundant components will use. For instance, in a 2*N* configuration, the redundant system can act as a hot standby (fully initialized backup), warm standby (partially initialized backup), or cold standby (uninitialized backup). A hot standby design can provide the fastest recovery but can also be more complex to design, since the standby node must maintain complete, up-to-the-moment state information about system activity.

In fact, design problems go beyond the redundant components themselves and extend to any applications communicating with those components. For instance, let's say a node provides compute services for client applications throughout the network. What happens if that compute node fails and another node, acting as a hot standby, takes over? Suddenly, those client applications must now all talk to a different node (the standby system).

With most OSs, achieving this *failover* can require careful design and network-specific code. But if the OS provides network-transparent Interprocess Communication (IPC), where applications don't effectively have to know which node they are talking to, then much of the effort and complexity of switching over to the redundant node disappears. In a distributed operating system like QNX Neutrino, for instance, accessing resources such as disks, file systems, and I/O ports on other nodes is so transparent that an application would need special code to know which node a resource resides on. From the application's perspective, then, there would be no real difference between talking to a primary or standby computer. See Figure 4.

Using more than one basket

The systems designer can also eliminate SPOFs by distributing applications and services across a cluster of loosely coupled CPUs, whether those CPUs reside in the same chassis or in physically separate machines. With a cluster, most services can continue running even if one node experiences catastrophic failure – it's a lot like putting your eggs in more than one basket. Clustering can also yield greater throughput, since each node adds its own CPU power, memory, I/O bandwidth, and so on.

Still, deciding which applications and hardware resources should be allocated to which node is a challenge all its own. In fact, it may be difficult to know until the integration phase whether processes and peripherals have been distributed in a way that provides optimal performance. The job is simplified, however, if the OS provides network-transparent IPC. For instance, applications could continue to access a disk drive even if that drive were moved to another node; no recoding would be required.

Out of the box?

HA demands a systems approach that encompasses everything from properly inspected solder joints to well-trained system administrators. Nonetheless, for most mission-critical applications, the cost of implementing HA is typically far less than the cost of the alternative: downtime. That's especially true today as more OS, board, and system vendors deliver HA features, thereby saving the systems designer from doing everything from scratch. HA itself may not come out of the box, but many of the tools to achieve it can.

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Website: www.qnx.com

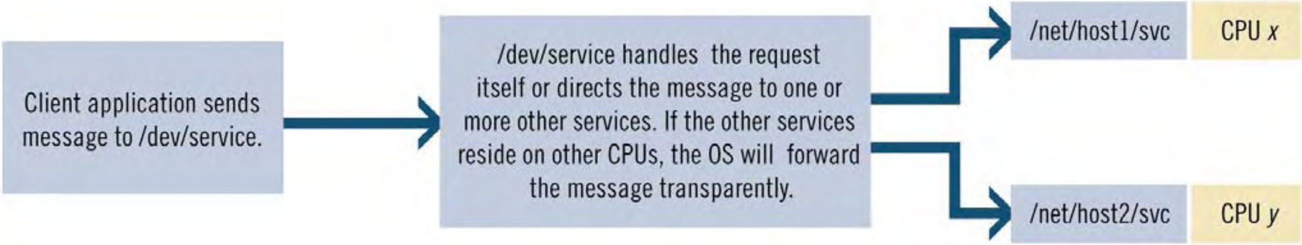

Figure 4

Rugged CompactPCI: Expanding choices and flexibility

By Thomas Roberts

Many of today's leading-edge embedded computing applications need solutions that can deliver uncompromised performance under difficult environmental conditions, including excessive heat, humidity, poor air quality, high altitude, shock, and vibration. Products designed to operate under some set of these environmental conditions are referred to as rugged, differentiating them from common commercial products. A challenge for application designers is that not all rugged products on the market are equal. Specifications can vary substantially because the term rugged has no industry-standard definition. One vendor's claim of ruggedness could be close to another vendor's commercial specification. In general, caveat emptor (buyer beware) applies and each application's specific environmental requirements must be carefully compared to the individual specifications of a potential product solution.

Before getting down to the product-selection level, it is useful to look at some general characteristics of rugged computing solutions and available options. Rugged characteristics can be divided into three areas:

- Excessive humidity
- Temperature extremes
- Shock and vibration

Humidity

Humidity is the simplest characteristic to understand and deal with. Computing systems in long term, high humidity situations are subject to molds and other types of spore growth. A variety of conformal coatings such as acrylic or urethane, which are applied at the board level, address these contaminants.

Temperature extremes

Rugged temperature extremes can be dealt with in a number of ways. The best method for a specific situation depends on factors such as the operating altitude, range of temperatures to be faced, and the platform's heat management capabilities.

Forced air from fans is the most common way to cool any computer. Some rugged systems simply use more air, from more powerful fans, to ensure that computer boards stay cool enough to operate. More sophisticated air-cooling techniques carefully direct additional air to the hottest components and enhance mixing between moving air layers. However, a suitable source of clean air might not be readily available during high-altitude operation or in sealed enclosures needed to guard against airborne contaminants such as dust and sand.

Excess heat can also be removed using liquid instead of air. Cool liquid can run through a cold plate next to the electronics, or spray cooling can take place inside a closed system. The spray cooling technique enables concentration of cooling exactly where it is needed, because liquid is sprayed directly onto the hot components. The heat dissipates when the liquid changes to vapor. However, spray cooling is not magic; the heat has to go somewhere so the vapor can be returned to liquid for continued spraying. A heat exchanger must be part of the system, with the heat removed from the other side of the exchanger by airflow, chilled water, or some other means.

One of the most popular methods for dealing with rugged temperature extremes is conduction cooling, which is a viable option at higher altitudes and in smaller spaces. Conduction-cooled boards draw the heat via solid materials from individual components to the chassis exterior. The exterior of the chassis can then be cooled by several different methods. When conduction cooling is used at lower altitudes to provide a compact, sealed environment, air cooling may work for the outside of the chassis. But when used at higher altitudes, the chassis is often cooled with a liquid.

An additional approach, which can be used in conjunction with any of the cooling techniques, is to employ components especially designed to operate reliably at higher temperatures. Using board components with a higher heat tolerance simplifies the overall problem of cooling the board.

Shock and vibration

Rugged systems often need enhanced mechanical integrity to withstand high shock and vibration forces at various frequencies. This usually takes the form of metal stiffening, most commonly around the edges of a computer board and sometimes across the surface or even embedded inside the board. At the chassis level, ruggedness is achieved by employing an isolator system, usually with two components, a spring to support the load and a damping element to dissipate the input energy.

Rugged advantages of CompactPCI

The CompactPCI standard offers a number of advantages to vendors developing rugged computing boards. First, CompactPCI boards are held firmly in place by their connectors, the guides on both sides, and a metal faceplate that screws or latches onto the card cage. Second, the pin and socket connectors are more reliable and have better shock and vibration characteristics than other form factors, such as PCI.

These characteristics give even a commercial-level CompactPCI board a certain level of inherent *ruggedness* for shock and vibration. Adding extra stiffening metal around the edges of a commercial CompactPCI card takes it to an even higher level of ruggedness, without requiring a board redesign. Putting edge-

stiffened boards in a rugged chassis results in a highly durable system, still compliant with the CompactPCI standard.

When dealing with extreme temperatures, the 3U CompactPCI form factor is especially well suited to conduction cooling. Edge-stiffening metal can be designed to also function as cooling rails, while the smaller 3U size means that, on average, electronic components are closer to those cooling rails. As the only 3U standard on the market with a reasonable number of user I/O pins available to the backplane, CompactPCI is in a unique position to satisfy the military requirement for modular COTS solutions in a small package.

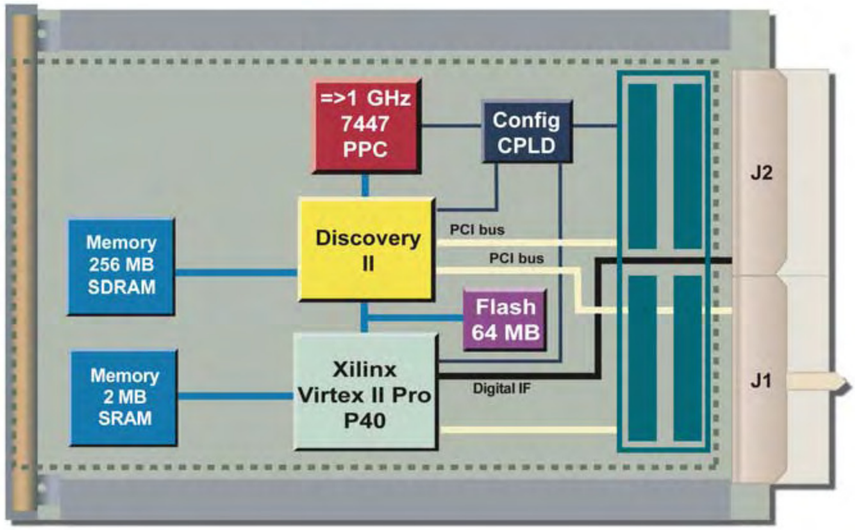

Figure 1

Rugged CompactPCI products expand steadily

The rugged advantages of CompactPCI, combined with the open-standard advantages of CompactPCI in general, have caused a steadily expanding number of rugged CompactPCI products to enter the market. The PICMG website lists 49 board vendors offering rugged CompactPCI products. Application designers facing harsh environments can choose from an array of products, supporting a variety of processor types and reaching different levels of ruggedization. Designers also have the flexibility to interface to many I/O types through combinations of direct onboard interfaces and mezzanine cards.

An example of innovative, rugged CompactPCI design

An example of this rugged flexibility is the MCP3 FCN from Mercury Computer Systems, delivering powerful signal processing capability in a space-efficient, 3U CompactPCI format. Fully capable of deployment in harsh environments, the MCP3 FCN module is available in both air-cooled and conduction-cooled versions. The conduction-cooled version is constructed with ruggedized mechanical casework that conducts heat to the edge of the board and also stiffens the board to withstand shock and vibration.

Processing density and efficiency for signal processing is achieved by combining a general purpose processor 1 GHz PowerPC 7447 and a Virtex II Pro P40 field programmable gate array (FPGA). See Figure 1. A Discovery II bridge chip connects these two processing units. Partitioning application software enables certain algorithms, such as fixed-point computations or non-data dependent operations, to go onto the FPGA. Other parts of the application, especially data-dependent operations, are targeted to the general purpose PowerPC 7447, which is easier to program for those types of algorithms. This style of application partitioning maximizes system performance and keeps overall development time manageable.

Three avenues for off-board communications and I/O are available via:

- The PCI bus on the J1 pins of the CompactPCI connector
- A digital Intermediate Frequency (IF) to the FPGA using a direct connection from a subset of the user-defined J2 pins
- The PMC, which can communicate directly with the FPGA or through the Discovery II chip to the PowerPC

To develop application components targeted for the PowerPC processor, engineers have access to a mature set of Mercury tools, including the Scientific Algorithm Library (SAL) with more than 600 routines optimized for the PowerPC. For those parts of the application that will run on the FPGA, developers can use the FPGA Developer's Kit (FDK). It is a collection of Mercury-developed Intellectual Property (IP), build files, command line tools, libraries, headers, drivers, board descriptors, diagnostics, and consulting support, all focused on helping engineers efficiently create reliable FPGA based applications.

Many options on the market

The following pages in the CompactPCI/MIL-STD Buyer's Guide list more than 90 currently available rugged CompactPCI products. User demands and exciting new technologies are both driving this dynamic market, insuring continued expansion of the list.

***Thomas Roberts** is a product marketing manager at Mercury Computer Systems, joining the company in 1999. He has more than 20 years of experience in systems engineering and technical marketing with IBM, Nixdorf, Data General, Digital Equipment, and Compaq. Tom has a BS in engineering from Cornell and an MBA from the University of Kansas.*

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199 Riverneck Road
Chelmsford, MA 01824-2820
Tel: 978-967-1291
Fax: 978-256-0852
E-mail: troberts@mc.com
Website: www.mc.com

MIL-STD: RUGGED COMPACTPCI CHASSIS, POWER, AND PROCESSOR BOARDS

	Chassis			Processor board									
COMPANY NAME/ MODEL NUMBER	Power supplies	With power	Without power	Pentium	Pentium II	Pentium III	Pentium 4	Pentium M	Power PC	RISC	Socket 7	x86	WEBSITE
Aborn													www.aborn.com.tw
Eric-151		•											
Absopulse Electronics													www.absopulse.com
PFC4500	•												
ACT/Technico													www.acttechnico.com
8751									•				
American Rugged Enclosures													www.areinc.com
Compact PCI Card Cage and Fan Assembly			•										
AP Labs													www.aplabs.com
FS-1260		•											
FS-1270		•											
FS-8705		•											
Applied Data Systems													www.applieddata.net
VGX										•			
Axiomtek													www.axiomtek.com
CPS6140		•											
Carlo Gavazzi CS													www.gavazzi-computing.com
709 Series Rugged Military Packaging			•										
714T Series		•											
Catapult													www.catapult.com
m500		•											
Cherokee International													www.cherokeellc.com
CMP/DMP 150 & 200	•												
Chroma ATE													www.chromaate.com
cPCI-5310		•											
Curtiss-Wright Embedded													www.cwcembedded.com
DPMC-106									•				
G4C – cPCI SBC									•				
Cyberchron													www.cyberchron.com
CVC-130		•											
Dawn VME Products													www.dawnvme.com
Model 710		•											
Ruggedized Chassis			•										
Dynatem													www.dynatem.com
CPC2						•							
ELMA Electronic													www.elma.com
11C08AD598Y3VB2X			•										

MIL-STD: RUGGED COMPACTPCI CHASSIS, POWER, AND PROCESSOR BOARDS

	Chassis			Processor board									
COMPANY NAME/ MODEL NUMBER	Power supplies	With power	Without power	Pentium	Pentium II	Pentium III	Pentium 4	Pentium M	Power PC	RISC	Socket 7	x86	WEBSITE
ELMA Electronic (continued)													www.elma.com
12R2 - 12U System			•										
12R2 - 5U System			•										
12R2 - 7U System			•										
12R2 - 9U System			•										
12R3 chassis		•											
2U Type 39			•										
Rugged-PCI 12R2		•											
Series D		•											
Type 12V NEBS			•										
Embedded Planet													www.embeddedplanet.com
EP8245M									•				
Fastwel													www.fastwel.com
CPC501								•					
General Dynamics													www.gdcanada.com
PC6010						•							
PC6300					•								
PSC6100	•												
GESPAC													www.gespac.ch
PCIPPC-2X									•				
PCIPPC-5									•				
Hybricon													www.hybricon.com
CompactPCI Power Planes	•												
Power Planes	•												
RME1221		•											
I-BUS													www.ibus.com
G0405/G0406		•											
ICP America													www.icpamerica.com
PAC-1000/1200		•											
PAC-1060		•											
PAC-700		•											
Integrated Power Systems													www.ipsi.net
5875	•												
JK microsystems													www.jkmicro.com
UFlashPLUS												•	
UFlashTCP-EP												•	

Continued on page 67

PMC Showcase

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info@pmcshowcase.com

ARINC 429

Curtiss-Wright Controls Embedded Computing

P429A ARINC PMC
ARINC 429 Comm. Controller

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- 64KB Dual Port RAM to support RS-485 DMA
- 8MB Flash Memory
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Curtiss-Wright Controls
Phone: (613) 254-5112
Fax: (613) 599-7777
E-mail: sales@cwcembedded.com
Web: www.cwcembedded.com

Telecommunications

adax

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- AAL2 SSAR/SSTED
- Dual OC3/STM1/STS-3c interfaces
- 4 T1/E1 trunks–software selectable
- Pre-integrated to 3rd party stacks
- New addition to Adax Signaling GW

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Fax: (510) 548-5526
E-mail: sales@adax.com
Web: www.adax.com

Compression/Decompression

Curtiss-Wright Controls Embedded Computing

Orion PMC
JPEG 2000 Video Compression/Decompression

- Real-time JPEG 2000 video compression and decompression
- Outputs two independent PAL or NTSC video channels
- Accepts up to 10 analog video inputs
- Full-frame rate encoding of standard 625-line PAL or 525-line NTSC video
- Available in PMC and PCI form factors

Curtiss-Wright Controls
Phone: (613) 254-5112
Fax: (613) 599-7777
E-mail: sales@cwcembedded.com
Web: www.cwcembedded.com

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High Density Signaling

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- 128 channels of multiple protocols
- LAPB/D/V5, FR, X.25 and HDLC
- Dynamically configurable
- Channelized controller
- 4 T1/E1 trunks–software selectable

Adax, Inc.
Phone: (510) 548-7047
Fax: (510) 548-5526
E-mail: sales@adax.com
Web: www.adax.com

TITAN

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Compression & Decompression

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- NTSC/PAL, S-Video, CVBS input
- Digital I/O, TV Out
- Custom options available

Titan Advanced Products and Design
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Fax: (858) 527-0150
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Web: www.titan.com

Front Panel Brackets

Purcell Technologies, Inc.

Front Panel Brackets

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Fax: 925-513-1370
E-mail: info@purcelltech.com
Web: www.purcelltech.com

Quad PMC Carrier

Zephyr Engineering Inc.

ZPCI.2900
64-bit/66 MHz Quad PMC Carrier

- Monarch CPU slot plus three IEEE P1386.1 PMC slots
- Dual speed clock generator automatically sets PCI bus speed to 66 or 33 MHz
- 1Mbyte of on-board socketed FLASH PROM
- On-board PCI bus arbiter
- Uses standard ATX power supply
- ATX I/O area accessible serial debug port

Zephyr Engineering, Inc.
Phone: (480) 736-8714
Fax: (480) 736-8322
E-mail: info@zpci.com
Web: www.zpci.com

Quad DSP PMC

BittWare

T2-PMC
Quad ADSP-TS201S TigerSHARC PMC Board

- 4 ADSP-TS201S TigerSHARC DSPs
- 14.4 GFLOPS processing power
- SharcFIN 64/66 PCI bus interface
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- 4GB/s ext. I/O throughput via ATLANTiS Architecture
- 256 MB SDRAM
- 8 MB Flash memory
- 8 500 Mbytes/sec link ports

BittWare, Inc.
Phone: (603) 226-0404
Fax: (603) 226-6667
E-mail: info@bittware.com
Web: www.bittware.com

Processor PMC (PrPMC)

MOTOROLA

PowerPMC-280
Processor Module

- Dual/single MPC7447 PowerPC® G4 processor up to 1 GHz with AltiVec™ technology
- Highly integrated Marvell Discovery II system controller
- Up to 1GB on-board ECC-protected DDR SDRAM
- Dual Gigabit Ethernet interfaces on PN4
- Up to 64MB user flash memory and 1MB boot flash
- PCI 2.2 interface: 64-bit/66 MHz

Embedded Communications Computing
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Fax: +1 602 438 3195
E-mail: inquiry@mcg.mot.com
Web: www.motorola.com/computing

MIL-STD: RUGGED COMPACTPCI CHASSIS, POWER, AND PROCESSOR BOARDS

	Chassis			Processor board									
COMPANY NAME/ MODEL NUMBER	Power supplies	With power	Without power	Pentium	Pentium II	Pentium III	Pentium 4	Pentium M	Power PC	RISC	Socket 7	x86	**WEBSITE**
Kinetic Computer													www.isci3000.com/kin/
PC/Ranger			•										
Kontron													www.kontron.com
CP301						•							
CP321									•				
CP604						•							
CP612											•		
CP620-PM									•				
Macrolink													www.macrolink.com
12-Slot VME and cPCI Chassis		•											
ML-1900 Series Leopard VII		•											
ML-1900 Series Panther		•											
ML-1900 Series Puma		•											
Mektron Systems													www.mektron.co.uk
CompactPCI Enclosures		•											
MEN Micro													www.menmicro.com
F2				•									
Mercury Computer Systems													www.mc.com
MCP3 FCN									•				
Motorola													www.motorola.com/computers
CPX2408/2408T		•											
North Atlantic Industries													www.naii.com
55PQ1	•												
One Stop Systems													www.onestopsystems.com
4U CompactPCI Enclosure		•											
4U-19S-2-350		•											
Performance Technologies													www.pt.com
ZT 6301	•												
ZT 6311	•												
Power Innovations													www.power-innovations.com
Q-RX Series	•												
Radstone Embedded Computing													www.radstone.com
EP1A-8240									•				
PPC4A									•				
SBS Technologies													www.sbs.com
AMC-cPCI 3000		•											

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MIL-STD: RUGGED COMPACTPCI CHASSIS, POWER, AND PROCESSOR BOARDS

	Chassis			Processor board									
COMPANY NAME/ MODEL NUMBER	Power supplies	With power	Without power	Pentium	Pentium II	Pentium III	Pentium 4	Pentium M	Power PC	RISC	Socket 7	x86	WEBSITE
SBS Technologies (continued)													www.sbs.com
CC7						•							
CK5									•				
CR7				•									
CR9								•					
CT8						•							
RL4									•				
Schaefer													www.schaeferpower.com
C4700 Series	•												
Schroff													www.schroff.us
20,000 Series			•										
europacPRO			•										
PEN-6105			•										
Pro Series			•										
SMA													www.SMAcomputers.com
Enduro												•	
Switching Power													www.switchpwr.com
CPCI-210Q-DC-47	•												
CPCI-350Q-P-38	•												
CPCI-350Q-P-47	•												
Synergy Microsystems													www.synergymicro.com
KYMD									•				
Technoland													www.technoland.com
TL-SBC 8000							•						
Thales													www.thalescomputers.com
CPU860-MD/MR/MM									•				
PMC860									•				
RA and RC PowerEngine7 SBCs									•				
Tracewell Systems													www.tracewellsystems.com
S33-1U			•										
S36-10U		•											
TPS600	•												
Transtech DSP													www.transtech-dsp.com
3CPF1									•				
Triple E													www.tripleease.com
MaxAir.10		•											
XTech													www.xtech-outside.com
Extruded Aluminum Enclosures			•										

NEW PRODUCTS

CompactPCI & AdvancedTCA

By Chad Lumsden

www.compactpci-systems.com/products

CHIPS & CORES: FPGA

Sundance

Website: www.sundance.com
Model: SMT351 **RSC No:** 20184
Embedded reconfigurable computing modules based on Xilinx Virtex-II Pro field programmable gate arrays (FPGA) • 1 Gigabyte of storage in DDR SDRAM (Samsung K4H511638B-GC / LB3 or Micron MT46V32M16FN -6) • Up to 400 MBps throughput rate • 32-bit data width • Single width module • Two Sundance High-Speed Bus (HSB) connectors with 60 I/O pins each • Eight Sundance Rocket Serial Links • Six 20 MBps communication ports • Xilinx Virtex-II Pro VP7 (optional VP20 or VP30) FPGAs • User defined pins for external connections (clock, trigger...) • Compatible with a wide range of Sundance Modules • TIM standard compatible • Weight approx. 58g

DATACOM: ETHERNET

DSS Networks

Website: www.dssnetworks.com
Model: 6267 SFP PCI-X **RSC No:** 20097
Pluggable fiber SFP connector options • Over 242 MBps per port / 490 MB total • Up to 1M frames per second • 133/100/66 PCI-X bus interface • Low profile form factor • Uses single 5V supply rail (optional 3.3V) • Onboard step-down regulators for core voltages • 3.8W total board power consumption • 0°C to 55°C ambient temperature • Supports Tornado 2.2 / VxWorks 5.5, Linux versions 2.4, 2.6, Embedded Linux

DEVELOPMENT PLATFORM

ACT/Technico

Website: www.acttechnico.com
Model: RAIDStor Develop. Kit **RSC No:** 20060
Contains everything needed to establish a complete Embedded Network Attached RAID solution with dual star topology in a PICMG 2.16 or VITA 31.1 enclosure • 19-inch rackmount chassis or tower with either PICMG 2.16 or VITA 31.1 backplane • Two RAIDStor 6200 storage blades, with up to 120 GB per blade • Two 10/100 or Gigabit Ethernet fabric switches • PICMG 2.16 or VITA 31.1 System/Node slot Pentium or PowerPC M single board computer • Includes any required Rear Transition Modules (RTMs) • Also includes a remote support package


RSC 20060

Pigeon Point Systems

Website: www.pigeonpoint.com
Model: BMR-H8S-ATCA **RSC No:** 20054
One of a series of IPM Sentry Board Management reference designs • Based on Renesas H8S/2168 microcontrollers • Specification compliant and interoperability tested • AdvancedTCA hot swap interfaces (handle and blue LED) • Hardware address detection from backplane • Payload power supply controls (multiple voltage levels) • Control of E-Keying governed fabric interfaces • Optional persistence of controls across IPM Controller resets • Dual redundant IPMB-0 • UART-based payload and serial debug interfaces • Thermal sensors (LM60 analog and/or DS75 digital) • Payload voltage monitoring • FRU LED management • Optional support for special purpose functionality • Core IPMC can fit in 28 mm x 30 mm footprint • All mandatory and many optional IPMI/AdvancedTCA commands supported over IPMB-0 • Numerous PPS extension commands, primarily used over the payload and debug serial interfaces • Serial interface protocol based on IPMI Terminal Mode • Payload alert notifications over payload interface for sensor events and receipt of reset/shutdown commands • Sophisticated support for firmware upgrades in the field • Simple but highly flexible configuration of firmware features

DSP RESOURCE BOARDS: COMPACTPCI

BittWare

Website: www.bittware.com
Model: T2-6U-cPCI **RSC No:** 20111
Two clusters of four ADSP-TS201 DSPs @ up to 600 MHz • 28.8 GFLOPS (3.6 GFLOPS of floating-point power per DSP) • 115 BOPS (14.4 BOPS of 16-bit processing per DSP) • 24 Mbits of on-chip RAM per DSP • Static superscalar architecture • Two Xilinx Virtex-II Pro FPGAs (XC2VP20/30) for I/O interfacing, routing, and coprocessing • ATLANTiS architecture featuring 9.6 GBps of external I/O throughput via Virtex-II Pro routing • 16 link ports @ up to 600 MBps each • 128 high-performance DIO (single-ended and/or LVDS) • 16 channels RocketIO high-speed serial transceivers (2.5 Gbps) • Two PMC sites with PMC+ extensions for BittWare's PMC+ I/O modules • 64-bit 66 MHz PCI interface via BittWare's SharcFIN PCI-DSP bridge • Up to 512 MB of on-board SDRAM • 16 MB of Flash memory for booting DSPs and FPGAs • Two link ports per DSP dedicated for interprocessor communications • Two link ports per DSP dedicated for I/O • 6U CompactPCI form factor • Complete software support, including remote control and debug, support for multiple run-time and host operating systems, and optimized function libraries

FIELDBUS: CAN

SMA

Website: www.SMAcomputers.com
Model: CCAN4 **RSC No:** 20095
Fourfold CAN module for the CompactPCI bus • 8 HP CompactPCI plug-in card • Insulation resistance 2.0k VAC/2.8k VDC • PICMG 2.0 R3.0 • Plug-in card carries four CAN2.0B compatible controllers of the SJA1000 kind • 64 byte FIFO • Support 11 and 29-bit identifiers at bit rates of up to 1 Mbps • 2.0k VAC/2.8k VDC between the CAN channels insulation resistance as well as towards the system • Rotary switch for the operation of multiple cards of the same type in one system, which is standard on SMA components • Complies with PICMG 2.0 R3.0 (32-bit bus, 33 MHz) 3.3V or 5V PCI signal voltages • European Railway Standard EN 50155 • Certified for use in the T3 extended temperature range (-25°C to +70°C, +85°C for ten minutes)

GATEWAYS

Zarlink Semiconductor

Website: www.zarlink.com
Model: ZL50031 TDM **RSC No:** 20191
Intended for carrier-grade applications that require high bandwidth switching capability • 4,096 x 2,048 switching between backplane and local streams • 2,048 x 2,048 switching among local streams • 2,048 x 2,048 switching among backplane streams • Rate conversion between backplane and local streams and among local streams • Backplane interface accepts data rates of 8.192 or 16.384 Mbps • Local interface accepts data rates of 2.048, 4.096 or 8.192 Mbps • Fully compliant to H.110 timing specification • Integrated PLL conforms to Telcordia GR-1244-CORE Stratum 4 Enhanced switching standard • Holdover Mode with holdover frequency stability of 0.07 ppm • Jitter attenuation from 1.52 Hz • Time Interval Error (TIE) correction • Master and Slave mode operation • Per-channel variable or constant throughput delay • Per-stream output advancement, programmable for backplane and local streams • PB-free package compatible with high and low temperature reflow

MASS STORAGE: RAID

ACT/Technico

Website: http://www.acttechnico.com
Model: RAIDStor **RSC No:** 20183
RAID 0, 0 + 1, and 1 + 1 configurable • Hot swappable • Dual star topology • Client/server model for storage access • Automatic and transparent duplication of the data across the primary and secondary storage blades • Smallest RAID footprint in the industry • Synchronization capability implemented between blades • Automatic failover • Diskless client boot support • Supports NFS, CIFS/SMB, Web Server, bootp, and FTP • Web Browser – Manage RAIDStor as an appliance or via SNMP • Link aggregation/failover implementation • Network management without impact to top level application speed

POWER SUPPLY

Picor

Website: www.picorpower.com
Model: QPI-4 Active EMI Filter **RSC No:** 20210
7 amp rating • 80 VDC (max input) • 100 VDC surge 100 ms • >40 dB CM attenuation at 250 kHz • >70 dB DM attenuation at 250 kHz • 1,500 VDC

hipot hold off to shield plane • 1.0" x 1.0" x 0.2" SiP (System-in-Package) • SMT Land Grid Array (LGA) • -40°C to 100°C PCB temperature • Efficiency >99% at full load

PROCESSOR BLADES

Continuous Computing

Website: www.ccpu.com
Model: LINUXblade XE20 **RSC No:** 20074
AdvancedTCA single board computer • Dual Low-Voltage (LV) next-generation Xeon processors, 3.67 GHz • 1 MB of L2 cache, 800 MHz processor chipset • Supports memory-intensive of 400 MHz DDR II 240 DIMM • Includes seven Gigabit Ethernet management, four USB 2.0 on private 64 bit 33/66/100/133 MHz • Supports Jn4/Pn4 to RTM • Support for Linux and VxWorks • PMC: Dual PCI-X 64 bit 66/100/133 MHz capable • Video: Analog RGB, ATI RageXL • Ethernet: 10/100/1000Base-T Ethernet Port, Intel 82540EM • Serial ATA: Dual Channels, Intel 6300ESB Quad • USB: USB 2.0 Ports, Intel 6300ESB • Serial ports: Three Ports, Intel 6300ESB, ITE IT8761E • Super I/O: ITE IT8761 E • IPMI controller: ATMEL ATMEGA128L/ATMEGA8L • Front panel I/O: Dual PMC, Analog RGB, Dual USB 2.0 ports, Gigabit management, dual serial ports

PROCESSOR: CELERON

Kontron

Website: www.kontron.com
Model: CP6500-V **RSC No:** 20120
Low voltage Celeron, Micro-FCBGA 478, 256 Kbyte L2 on-die cache • 400 MHz ULV Celeron ultra low power dissipation • 1 GHz LV Celeron high performance • All processor versions with passive heat sink • Depending on the processor version forced air cooling at a specific flow rate might be required in the chassis • 100 MHz memory speed, Intel 82815 GMCH • Up to 512 MB SDRAM memory without ECC on one 144-pin SODIMM socket, smallest memory size 128 MB onboard 2.5" HDD mounting CompactFlash socket Type II 1 MB Firmware Hub for BIOS 8 Kbyte EEPROM for CMOS data storing (for no-battery operation) supervisory functions, clock/calendar watchdog, software configurable, 125 msec to 256 sec in 12 steps, generates IRQ, NMI, or hardware reset, two stage configuration for NMI and Reset Hardware monitor Winbond W83627 for thermal control, fan speed, and all onboard voltages

PROCESSOR: PENTIUM III

MEN Micro

Website: www.menmicro.com
Model: EM07 **RSC No:** 20092
A complete embedded SBC for use on any carrier board in different industrial environments • ULP Pentium III / 933 MHz ULV Celeron • Up to 650 MHz • Up to 512 MB DRAM • CompactFlash • Dual Fast Ethernet • COM 1 (front) • Optional COM 2 (front) • Graphics (rear) • 2 USB 1.1 (rear), (E)IDE (rear) • FPGA-programmable I/O functions (rear) • Stackable with PCI-104

PROCESSOR: PENTIUM M

Continuous Computing

Website: http://www.gocct.com/
Model: PP 312/012 **RSC No:** 20182
2.0 GHz or 1.8 GHz Intel Pentium M processor • Up to 533 MHz Front Side Bus, 64 Kbytes L1 cache, 2 Mbytes L2 cache, no CPU fan needed low power processor 1.6 GHz and 1.1 GHz processor versions available • Up to 2 Gbytes of DDR DRAM (with ECC) • Two PMC module interfaces (32/64-bit at 33/66 MHz) • High performance EIDE interfaces with optional onboard disk drive or optional CompactFlash/Microdrive interface • Two 10/100/1000Mbps Ethernet interfaces, Dual Gigabit Packet Switching Backplane (PICMG 2.16) • One USB port, 32 Mbytes of Application Flash EPROM, 512 Kbytes of BIOS Flash EPROM, 512 Kbytes of battery backed SRAM • CompactPCI controller • Operates in system slot or peripheral slot, 32/64-bit at 33/66 MHz CompactPCI interface, Option to bypass CompactPCI bus (Satellite Mode), IPMI (Intelligent Platform Management Interface) • PICMG 2.9 (System Management Specification) • Graphics interface, keyboard, and mouse interfaces • Watchdog timer and Long Duration Timer • Up to three RS-232 serial channel interfaces: 1 or 2 onboard, 2 on Optional Transition Module • Optional Transition Module for rear panel I/O • Two RS-232 channels, parallel printer port, and floppy disk interfaces included

For further information, enter the product's RSC# at www.compactpci-systems.com/rsc

NEW PRODUCTS

Kontron

Website: www.kontron.com
Model: AM4001 **RSC No:** 20053
AdvancedMC module • Pentium M up to 2.0 GHz • Max. 4 GB memory • Single width, half/full height • AMC.0/.1/.2/.3 compliant • PCI Express interface • 2 GigE 1000Base-BX (SerDes) ports

PROCESSOR: POWERPC

Artesyn Communication

Website: www.artesyncp.com
Model: PmPPC7447 **RSC No:** 20107
Up to 1.3 GHz PowerPC MPC7447A processor • Up to 2 GB SDRAM in SODIMM packaging • Marvell Discovery III system controller • Dual 10/100/1000 Ethernet with P14 access • 10/100 Ethernet on front bezel • I2C and 4 GPIO ports with P14 access • Linux 2.4.22 and VxWorks 5.5 BSPs • RoHS/WEEE compliant configuration available in 2006 • Quality assured by over 30 years of design experience and a TL-9000 and ISO 9001:2000 certified quality management system

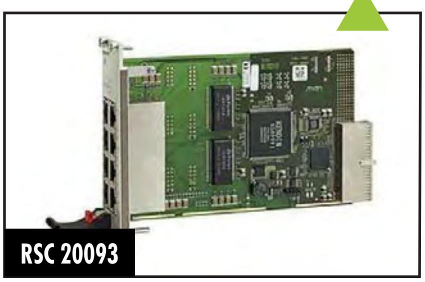
Extreme Engineering

Website: www.xes-inc.com
Model: XPedite1032 **RSC No:** 20072
PowerPC 440GX 533-800 MHz processor • Conduction cooled 3U CompactPCI card • One conduction cooled PMC (CCPMC) slot • Extended shock and vibration tolerance • Up to 256 MB 266 MHz DDR SDRAM • 128 MB soldered Flash • Two 10/100/1000 Mbps Ethernet ports • Two RS-232 serial ports • Backplane I/O • Integrated 256 KB SRAM or L2 cache • VxWorks Driver and BSP

ROUTERS/SWITCHES

MEN Micro

Website: www.menmicro.com
Model: F301 **RSC No:** 20093
3U Fast Ethernet Switch module for rugged mobile communication systems • 8 HP 32-bit/33-MHz CompactPCI • Up to 8 Fast Ethernet ports (front) • 1 FastEthernet controller (rear J1) • Option: 1 Fast Ethernet port (rear J2) • -40°C to +85°C operating temperature



Radstone Embedded Computing

Website: www.radstone.com
Model: GS16 **RSC No:** 20126
Fully rugged, standalone Gigabit Ethernet switch • IPv6-capable • 16 1000/100/10 Mbps ports; 32 Gbps non-blocking fabric • Optionally available 12-port optical expansion capability • Fully Layer 2 and Layer 3 managed • IP68-rated front panel connectors • Easily modifiable front panel for varying connector types • -40°C to +55°C conduction-cooled operation at the thermal interface

SERVERS

NextCom

Website: www.nextcomputing.com
Model: NextBook Series **RSC No:** 20029
Single Intel P4 processors from 3 GHz to 3.8 GHz • 15" SXGA+ or 17" WSXGA+ LCD display • Server architecture: 800 MHz Front Side Bus, ATA100" HDDs • Optional RAID0 or RAID1 second HDD • High performance graphics: AGPx8 ATI Mobility • Radeon 9700 or PCI Express • 16x Radeon X800 Single Gigabit Ethernet port (10/100/1000 • High performance memory DDR or DDR-2 to 3 GB • Internal optical drive (DVD, CDRW-DVD, or DVDRW)

STORAGE

Adtron

Website: www.adtron.com
Model: EA8R **RSC No:** 20189
Storage network support • Using iSCSI over high speed GigE interface with the well-established SCSI command set permits the ability to manage data storage and retrieval with support for multiple hosts • Dual GigE interface • Shelf redundancy: redundant ports on the backplane provide two paths to the storage blade • AdvancedTCA form factor • ActiveRAID technology: Onboard management ensures Host CPU and applications are not impacted by RAID functions or blade failures • Enterprise-class 2.5-inch hard disk drives • High performance and provides 100% duty cycles in RAID operations • Serviceability: Removable front panel provides easy access to each individual drive in event of a drive failure • Disk level Hot Swap - High reliability; the shelf continues to function until the impaired disk is replaced • Board level Hot Swap: Out-of-service storage blade can be removed and replaced without impacting shelf operation

SWITCH

Diversified Technology

Website: www.dtims.com
Model: ATS1460 **RSC No:** 20124
24 port Gigabit Ethernet base fabric L2/L3 switch • 24 port Gigabit Ethernet expansion fabric L2/L3 switch • 16 port 1Gb/2Gb Fibre channel switch • Fully managed solution with SNMP, CLI, Web interface, and Telnet/SSH • Wire speed non-blocking performance on all 3 switches • High Availability through redundant hub and shelf manager support

DSS Networks

Website: www.dssnetworks.com
Model: CPCI 2.16 8261 **RSC No:** 20099
12-port Gigabit Ethernet switch blade • 12 ports of 10/100/1000Base-T Gigabit Ethernet over copper with 2 1000Base-SX/LX fiber uplinks • PICMG 2.16 6U fabric card compliant • Compatible with both standard CompactPCI and PICMG 2.16 backplanes • All 12 ports may be routed to slots on the CompactPCI backplane or externally via rear I/O • Up to two fabric boards may be used per chassis for a total of 24 ports • System management interface supported via the PICMG 2.9 IPMI interface • Optional two 1000 base SX/LX gigabit fiber ports with standard SFF LC connectors via the front panel • Onboard RISC/DSP processor for local management • Operates as a standalone or fully managed switch • LEDS for each port showing link status, transmit and receive, and link quality • All LEDS are multifunction and can be used for additional functions including cable testing and energy detection • PICMG 2.1 R2.0 hot-swap compliant

TEST SYSTEMS

Applied Dynamics Int'l

Website: www.adi.com
Model: rtX **RSC No:** 20199
High performance real-time simulation using standard PC technology • QNX POSIX-compliant real-time operating system • Supports popular commercially available I/O boards in PCI, PXI, IP, and PMC form factor • Supports popular simulation languages including Simulink, SystemBuild, Statemate, AMESIM, Dymola, C/C++, Fortran, ADSIM • Uses Intel Pentium and AMD Opteron processors as single and multiprocessor models • Uses the ADvantage simulation framework including ADvantageVI, ADvantageDE, and ADvantage

TURNKEY SYSTEM

TietoEnator

Website: www.tietoenator.com
Model: Stack-on-a-Card **RSC No:** 20027
Fully embedded signaling solution • Protocols: MTP, SCCP, TCAP, MAP, ANSI-41, INAP, BSSAP, CAP and ISUP in compliance with ITU, ANSI, TTC, and Chinese SS7 standards • SIGTRAN in compliance with IETF standards, M3UA (RFC 3332 and 3GPP TS 29.202) and SCTP (RFC2960 & RFC 3309) • Access to SS7 protocols through distributed easy-to-use APIs that are linked together with the application • Thread-safe, callback C/C++ protocol APIs available for Sun Solaris, Windows NT, Windows 2000, Red Hat Enterprise Linux, HP-UX, and IBM AIX in application host environment • Possibility for multiple applications to use the same protocol stack • Link capacity extension without installing new communication boards or rebooting the system • Management support in host environment • Graphical Java-based configuration tool • Standalone or High-Availability configuration (one or two controller boards) • Four 1.5/2 Mbps E1, T1, and J1 front-panel interfaces with up to 64 links per controller board • Optional 4-port 10/100 Mbps Ethernet interface dedicated for SIGTRAN • Up to 512 SCTP associations New functionality in version R2: • TTC (Japan) and Chinese stacks • Mixed stacks: ITU application parts over ANSI SCCP/MTP, ANSI application parts over ITU SCCP/MTP

For further information, enter the product's RSC# at www.compactpci-systems.com/rsc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